STARHAWK

by Cinematronics

TM

SERVICE AND OWNERS MANUAL

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STARHAWK SERVICE

AND

OWNER'S MANUAL

CONTENTS

WARRANTY FOR STARHAWK

Cinematronics, Inc. warrants the goods to be free from defects in materials and workmanship under normal use and service for a period of ninety (90) days from the date of delivery on all parts except switches, potentiometers, buttons, fuses and lights, for which the warranty period is thirty (30) days from the date of delivery. Cinematronics makes no representation or warranties concerning the goods whether express or implied by operation of law or otherwise, including those of merchantability or fitness by operation of law or otherwise, including those of merchantability or fitness for any particular purpose, or with respect of patent infringement, except as may be specifically made herein, to the repair or replacement of such parts which have been returned to Cinematronics plant at purchaser's expense and which examination shall disclose to Cinematronics satisfaction to have been so defective and to be the shipment of such repaired or replacement parts to the purchaser F.O.B. the shipper point.

This warranty does not apply to any Cinematronics product which has been altered or repaired by unauthorized personnel or service facilities or any products which have had the unit serial number altered or removed.

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GENERAL INFORMATION

Generally speaking, your Starhawk game is designed much the same as conventional video games. The only major exception to this is the fact that the Starhawk game is provided with an alternate means of visual display: the patented Vectorbeam tm* monitoring system.

The game is, however, built of the same basic building blocks as any other video game.

The Power Supply, which provides all necessary voltages to power each separate electronics assembly as well as all lighting required throughout the game. It must be noted that there are "on board" regulators provided for certain voltages needed on both the audio logic board and the display printed circuit board. The plus five (+5) volts d.c. regulated voltage for the central processing logic board (CPU) is developed totally on the power supply. This same voltage is used where needed on the audio logic board and also the display printed circuit board.

The Central Processing Unit, contains circuitry to strobe and interpret all input functions including the player control panel switches and all coin and credit information and to create all the digital signals used in providing the visual display. It also contains all the software (i.e., machine language and game personality memory) needed to control the game operation and to generate the proper vectors needed to display.

In fact, the CPU logic board contains a great portion of the vector generating system, which also includes the display unit. The CPU logic board also controls the switching (electrically) of the audio printed circuit board.

*Vectorbeam tm is Cinematronic's service mark for video game repair and educational services.

The Audio Board, as in many other video games, is comprised of a noise generator and the associated wave shaping circuits as well as a number of amplifier stages on command from the CPU logic board.

The Vectorbeam tm * Display Electronics is the final form of interpretation of the CPU's calculations. The CPU logic informs the display electronics unit of information regarding line length and line placement on the CRT. This is accomplished with two twelve-bit words, one each for horizontal and vertical deflection, and a number of other controlling signals for the cathode drive circuit and switching in the delfection circuits.

The major difference between the vector generator and raster scan type monitors is the means by which the cathode beam is directed (deflection) across the screen.

In the raster scan types of display the electron beam from the cathode to the anode of the CRT is constantly deflected (scanned) across the face of the CRT is a series of horizontal lines that trace from the upper portion of the screen to the bottom in a syncronous pattern. Vertical information is added, also syncronous with the horizontal, forming a matrix-type pattern of mathematically possible illumination points on the CRT. If the cathode current is increased at these points on the screen in matrix-type patterns (similar to placing dots on a piece of graph paper where the lines intersect) coherent video in the form of shapes and alpha-numerics to form the game backgrounds can be displayed.

The vector generator takes a slightly different approach to cathode beam deflection. The results are a much higher degree of resolution and much smoother motion across the screen, as well as the ability to draw true

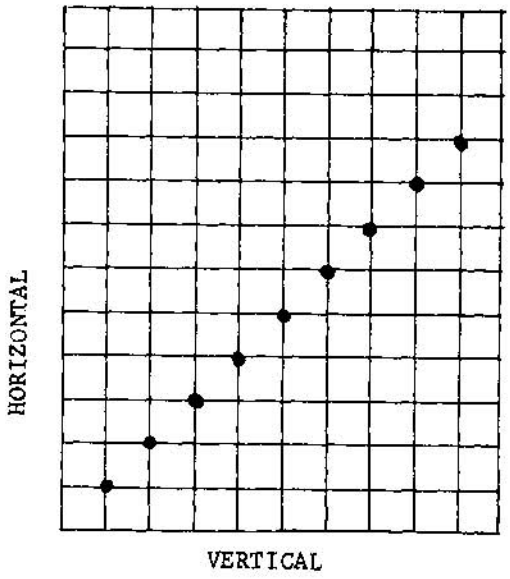
curved lines on the screen. Rather than using a constantly scanning cathode beam, the beam is directed only to points of eventual illumination, using a vectoring form of programming rather than a matrix approach. Basically, the cathode beam is directed between two determined points, and illuminates the entire path of phosphores between these two points, unless blanked by stopping cathode current (i.e., when the beam moves from one star to another on your screen). The ability to illuminate the entire path of phosphors crossed by the electron beam, in any direction desired, (which is not possible in a raster scan system) creates a much higher degree of resolution than can be found in a raster scan system while at the same time creating a much greater number of angle possibilities. This is also supported by the ability to accomodate two twelve-bit words of information, twelve each for vertical and horizontal deflection, and the fact that there is no background illumination from a constantly scanning beam when brightness is turned up. The higher degree of resolution combines with the totally blackened background creating an appearance of depth not found in a raster scan system.

Another major design difference is the fact that no sync. signals are needed to produce vectors on the CRT. This greatly simplifies the hardware design of the system, and therefore the understanding of the theory of operation, of the CPU logic as well as the display electronics.

VECTOR THEORY

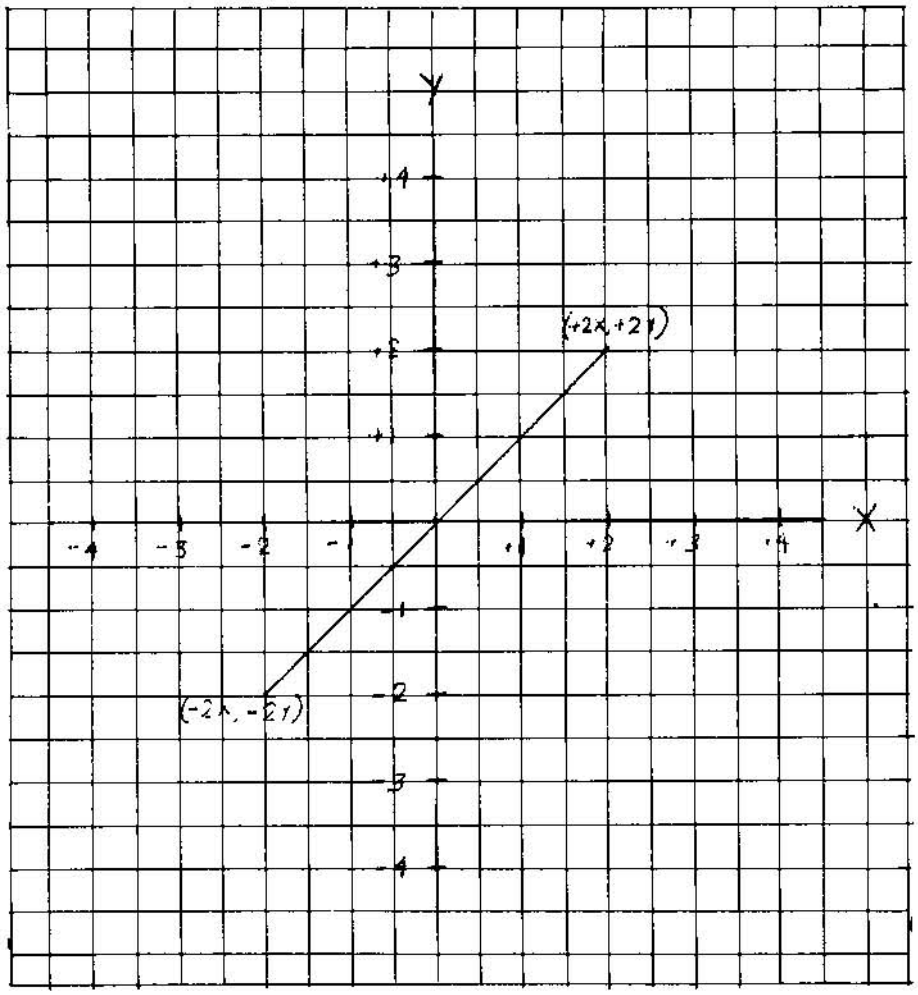
In order to understand the basic concept behind a vector generated display, it is important to have a basic knowledge of vector theory.

As mentioned in the general information section of this manual, the raster scan display uses a matrix type display pattern. A graphical representation of a matrix is shown below in Figure A.



For example, to produce a line on the CRT with a matrix-type pattern, the appropriate intersection points of horizontal and vertical lines are illuminated. The calculations which select these points are made on the logic board, and converted into video information for the monitor to digest. Although there are spaces between the illuminated points, the illusion of a solid line is made by your eyes, and the resolution is determined by the number of available horizontal and vertical lines in the system, and the speed of the sweep.

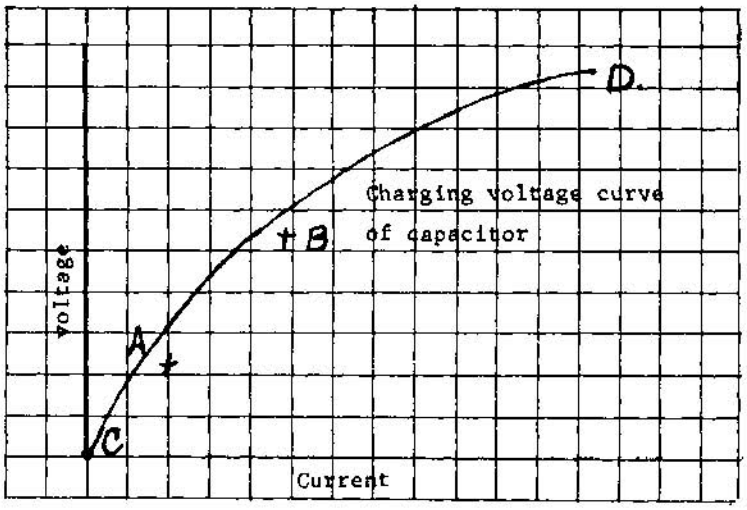
In the vector display system, there are no horizontal and vertical lines (no sweep) or sync. a line created using a vector system as shown in Figure B., below.



A line is drawn by programming a beginning and ending point of the line to be drawn, and forcing the cathode beam to travel between these two points, illuminating the entire path of phosphorus on the CRT. The angle of the line, the position of the line, and the length of the line are determined simultaneously, and simply, by selecting the proper voltage levels for the beginning and ending points of the line.

This is accomplished by the two twelve-bit codes (words) applied to the DAC-80's on the display board. The DAC-80 will produce a different voltage level at its output for each possible combination of input levels (of which there are 4128 possibilities for each 12 bit word.)

It is also important to remember the function of the LF 1331D (V-2) analog switch and its output RC network (see monitor theory). Because we are dealing with reactive components in C101 and C201 on the display board, the charging voltages found are non-linear by nature. (See Figure C., below).



Therefore, when a line appears on the CRT, it is actually only part (section A-B, Figure C) of the entire path taken between the beginning and ending points of the vector (C-D). The section of A-B is chosen as the most linear portion of the charge curve, and illuminated

Sections C-A and B-D are blanked at the cathode, and points A and B chosen by controlling the analog switch (V-1) on the display board. Again, these calculations are all performed on the CPU logic board.

The end result of using the vector generator is an immensely increased number of programable point, which is in direct proportion to the word size and the capabilities of the DAC-80 (i.e., greater esolution, definition and smoother motion using minimum of hardware).

CPU BOARD

The processor hardware can be broken down into five basic functional blocks as shown in Figure 1. The arrows indicate the possible data flow directions between the various blocks. The ALU and Control block are the main components of the processor while the Memory and I/O blocks may be thought of as merely peripherals. Figure 2 is a detailed block diagram of the processor. The numbers in each block correspond to the entires in Table 1, which lists the IC numbers of the main components of each functional block.

The following is a brief description of each block shown in Figure 1. The numbers beside each functional block name are the numbers in Figure 2 which correspond to a particular function.

RAM (6)

The RAM is implemented with three 9101C read/write static memories configured as a 256 x 12 bit block. Data can be transfered to or from this memory via the ALU block. The processor uses this RAM as a scratch pad.

ROM (10)

The ROM is configured as an 8k x 8 bit block of memory. These memory locations contain the program instructions and/or data. It is accessed via the processor control unit.

IO 19, 17, 18

The I/O block consists of 8 input lines implemented with a bit addressable latch, 24 input lines implemented with data selectors, and two 12 bit registors which are connected to the X Y display deflection circuits via D/A convertors.

Arithmetic Unit 1,2,3,4,5

The arithmetic unit performs all the arithmetic processing for the system. It consists primarily of two 12 bit accumulators, an arithmetic logic unit and various data selectors. The accumulators can function as temporary storage registers for arithmetic calculations, or as the source and destination registers for I/O operations. The ALU performs the actual arithmetic functions upon the data in the accumulators. The data selectors are used to select the various sources of data which will be processed.

Control Unit (15, 16, 14, 7, 8, 9, 11, 12, 13)

The control unit is the heart of the processor. It performs all instruction decoding operations and generates all the necessary control signals which the rest of the hardware requires to function correctly.

The following is a discussion of each block shown in Figure 2.

1. Accumulator Selector

The accumulator selector consists of 3 quad data selectors. They are used to select the output of either the primary or secondary accumulaotr for processing by various other sections of the system.

2. & 3. Primary and Secondary Accumulators

The two 12 bit accumulators are implemented with quad bidirectional shift registers. The primary accumulator consists of S4, P4, M4. The secondary accumulator consists of T4, R4, N4. All data manipulation in the processor is accomplished using these two accumulators. All output data flows through these registers.

4. Arithmetic Logic Unit (ALU)

The ALU is used to perform all necessary arithmetic functions within the processor. The ALU is implemented using three 25LS181 (N6,M6,L6) function

generators, three 74LS85 (N9 M9, L9) 4 bit magnitude comparators, and a 74S182 (L4) look ahead carray generator. The data which the ALU manipulates can come from four different sources. The first source is the contents of the accumulators via the accumulator selector. The second and third sources are the ROM and RAM data outputs via the ALU data selector (N11, M11, L11) and the fourth source is the external input lines via the input selector (E4, D4, C4).

5. Data Selector

The data selector is used to read data into the ALU from either the RAM or ROM memory. Note that the ROM data is only 8 bits wide while the RAM data is 12 bits wide.

6. RAM Storage

The system RAM consists of three 9101C high speed static memory chips connected as a 256 x 12 bit block. The block is 12 bits wide in order to allow the contents of an accumulator to be stored. The processor uses the RAM as temporary storage of program variables, data pointers or any other data of a dynamic nature.

7. RAM Address Selector/Register.

The output of this register is tied directly to the address lines of the RAM. It consists of a multiplexer which routes address data from either the ROM or RAM locations to the RAM address lines. The capability to use RAM data to select RAM addresses is the basis for the indirect addressing mode of the processor.

8. Page Selector

The page selector is used to latch the high order 4 bits of a RAM address during some types of RAM access instructions.

9. ROM Data Register

This register is used to temporarily hold data from the ROM during an instruction fetch.

10. ROM Memory

The ROM memory consists of the actual memory chips plus a data selector and latch circuit. The latch is used to improve the memory access time during a two byte instruction fetch by allowing one byte of the instruction to be latched while the RAM address lines are decoded for the other byte. The data selector can then be used to rapidly access both bytes of the instruction b y switching between the latch and memory outputs.

11. Instruction Register

The instruction register is a latch which holds the current op code as read from the ROM. Its output is tied to the instruction decode circuitry which in turn generates the necessary signals to execute the instruction.

12. System Sequencer

The system sequencer is used to decode an instruction op code and to generate the appropriate timed sequence of signals which execute the instruction. The op code is decoded by suing it as the address data to a set of decoder ROMS. The outputs of the decoder ROMS are then synchronized with the system clock and used to control the various system functional blocks.

13. Line Length Counter

The line length counter is used during the process of drawing a vector to control the length of a vector, by turning off the beam at a pre-determined time after the vector is initiated. The counter is loaded with a value from a line length ROM and then counts up until it overflows which in turn generates a signal to indicate the vector has been finished.

14. Program Address Selector

This selector is used to provide the address data to the program ROM. It selects either the program address counter output or the accumulator selector output and routes this data to the ROM address lines. The ability to use the accumulator contents as address data allows the program to randomly access data tables stored in the ROM or to compute a branch address after a conditional test.

15. Program Address Counter

This is a 12 bit counter whose output defines the next location in ROM to be accessed. It is normally clocked sequentially to step through a program. However, it can be loaded with data from the program address register which is how the jump instructions are implemented.

16. Program Address-Register

This register is a latch used for temporary storage of an address which will be loaded into the program counter during a jump instruction. The input data to this latch can come from either the program ROM or the scratch-pad RAM.

17. Input Selector

The input selector is used to read the state of one of the 24 input lines into the selected accumulator. There are 16 primary inputs and 8 secondary inputs. During an input instruction the upper 11 bits of the accumulator are set to zero while the least significant bit reflects the state of the input line. All input lines have pull up resistors on them so that they will read high if they are left unconnected.

18. Output Selector

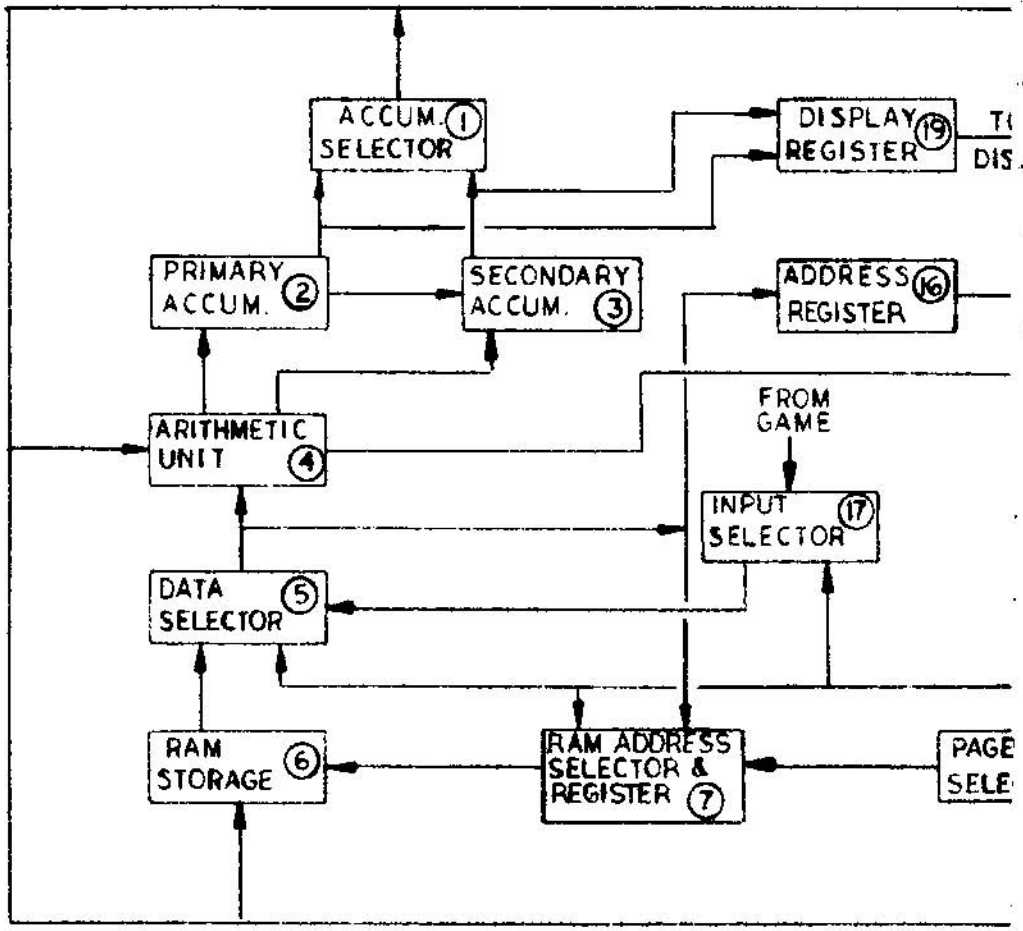
The output selector is a bit addressable latch used to control the 8 output lines. During an output instruction the selected output line is set to the complement of the least significant bit of the accumulator. The output lines are used to control the audio board, display intens ty and the mechanical coin counter.

19. Display Registers

The display registers are the interface between the processor and the display driver circuits. These registers are latches into which the contents of the accumulators can be stored. The outputs are tied to D/A converters which provide the input voltage to the display deflection amplifiers.

BLOCK NUMBERS AND COMPONENT I.C.'S

1. T-2, R-2, N-2
2. S-4,P-4, M-4
3. T-4, R-4, N-4
4. N-6, M-6, L-6, N-9, M-9, L-9
5. N-11, M-11, L-11
6. N-14, M-14, L-14
7. J-12, I-12
8. H-12
9. S-13
10. U-7, R-7, T-7, P-7, U-9, T-9, U-11, T-11
11. T-13
12. A-8, G-10, F-10, G-14, F-14, E-14, D-14, C-14
13. E-6, D-6, C-6, E-8, H-8, G-8, F-8
14. S-9, R-9, P-9
15. S-11, R-11, P-11
16. P-13, R-13
17. E-4, D-4, C-4
18. F-2
19. S-2, P-2, M-2



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REVISIONS			
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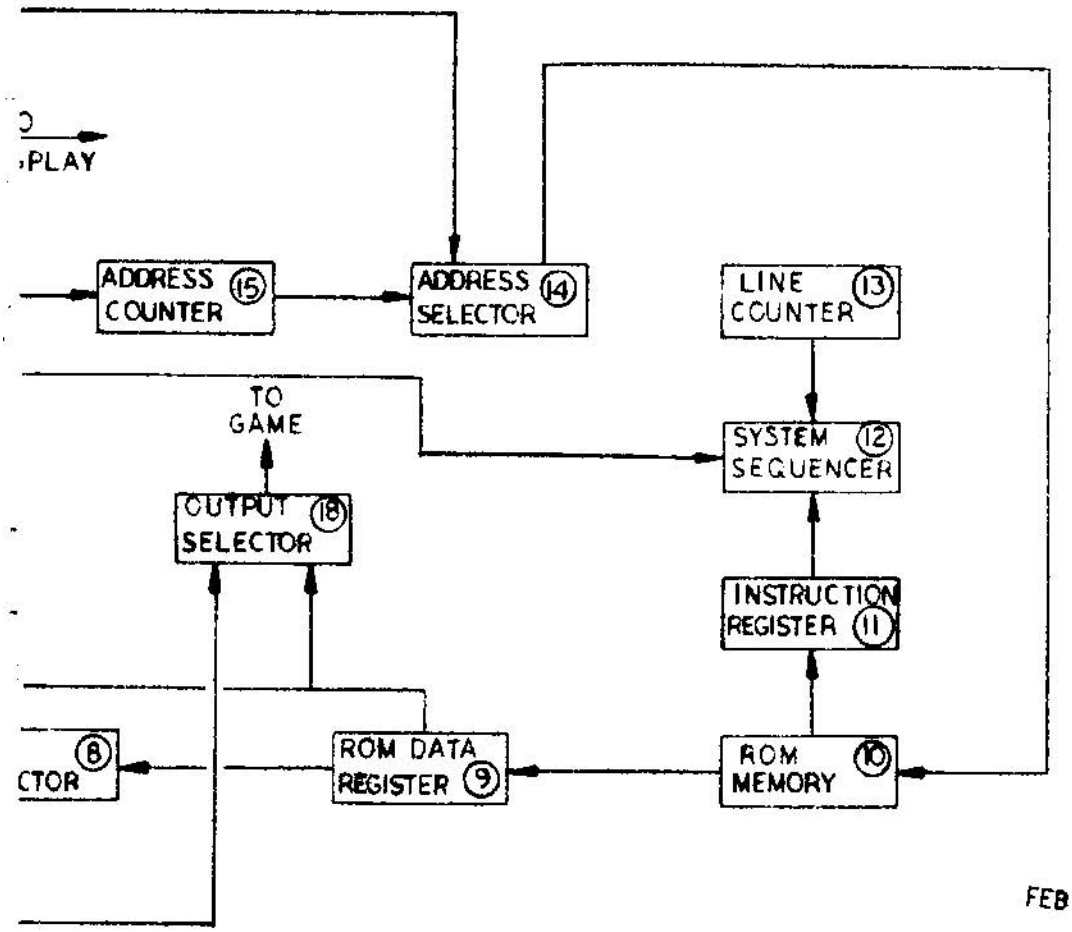

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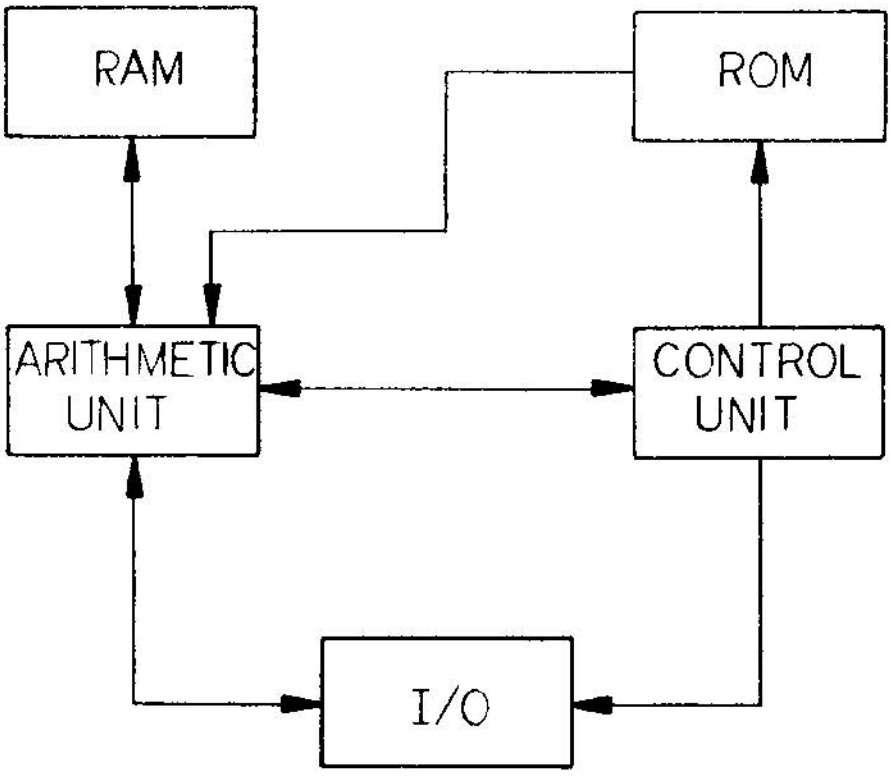

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MATERIAL:	DRAWN BY: S. HURLBERT	DATE 2.79	CINEMATRONICS INC.	El Cajon Ca. 92020
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	TOLERANCE: UNLESS OTHERWISE SPECIFIED		MODEL NO.	DWG SIZE A / DWG NO. BD201000 / REV.
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STARHAWK AUDIO BOARD

The Starhawk audio board is a self-contained electronic sound generation system that requires connections only to external power, control, and loudspeaker connections. Sounds generated include a simulated explosion, laser firing sound, and a special FMed waveform used in association with the killer ship.

The circuit incorporates a master on/off control, pin 15 of the control connector. When this pin is at a high level, the board is disabled and no audio is produced. When this pin is at a low level, the board is enabled and can produce under digital control, any or all of the sounds listed above. In addition, anytime that the board is enabled it produces a low level background noise.

The laser firing sounds are produced by two completely independent circuits so that either or both channels may be active at any time. The channels, pins 12 and 13, are turned on by a high input level and will produce sound continuously so long as the input remains high. The sound produced starts at a high pitch and decreases in frequency with time until it stabilizes at a very low frequency. Time constants in this circuit have been chosen for best performance with a one second duration control signal. When the control signal returns to a low level, the circuit resets within 150 microseconds and is then ready to be retriggered.

The explosion sound consists of digitally synthosized noise with a large amount of low frequency power. The explosion is triggered by a low-going pulse on Pin 11.

Triggering will occur on pulse durations as short as 100ns, but is designed to be done by pulses of 400ns or more. Maximum trigger pulse length should be limited to approximately 30ms, since the logic may start timing the duration of the explosion from the end of the trigger signal, rather than the start (this is a characteristic of the 556 IC used).

The killer ship sound has two control lines, pins 14 and 16. Pin 14 is the on/off control (high level off). This sound is intended to be used by setting Pin 16 high, waiting one second, and then setting both pins low. This creates a warbling sound that starts at a low pitch, ramps up to a high pitch before turning off.

THEORY OF OPERATION

Output Amplifier

The audio power output amplifier uses a conventional operational amplifier (op amp), with a current booster connected to its output. The circuit is connected as an inverting amplifier with variable gain obtained by the use of a variable resistor in the feedback path. The input to the circuit is coupled through an electronic switch which serves as the master on/off control. The maximum possible output level is limited to approximately plus or minus 12 volts by saturation in the op amp's output stages. For best results, the volume control should be set below the point where saturation occurs. The circuit can drive an 8 ohm loudspeaker to approximately 8 watts RMS power.

Laser Firing Sound

The laser firing sound generators each use identical circuitry. Four basic elements are used in each channel: a voltage controlled oscillator (VCO), a binary counter, a read only memory (ROM), and a digital to analog converter, (DAC). Two logic inverters are used to enable/disable the channel,

and to generate the control voltage for the VCO.

In standby, the control input level is low, forcing the first inverter's output high which both disables the ROM through it's chipselect input and also causes the second inverter's output to pull low, which discharges the capacitor connected to it. Since the ROM is disabled, it produces no output to the DAC, which produces no signal to the audio output stage. The VCO will be operating at maximum frequency because its control voltage is minimum. (see below for detailed VCO operation description).

When the laser firing sound is enabled, the ROM's chip enable is activated, allowing it to produce a binary output signal. This signal is connected directly to the DAC (the 4 resistors), which converts the binary data on it's input to an analog signal level at its output (the junction of all the resistors). Simultaneously, the output of the second inverter goes high (open), removing the short across the capacitor. The capacitor will now be slowly charged in a positive direction, a little bit of charge being accumulated on each positive cycle of the oscillator's output. As the voltage on this capacitor rises, the frequency of the oscillator decreases, reducing the pitch of the generated sound.

The oscillator's output signal is buffered by a transistor and an inverter, and is then applied to the input of a 7 stage binary counter. The binary counter presents its output directly to the ROM, which converts each of the 128 possible counter states to a particular data output corresponding to each state. The data stored in the ROM produces a rough waveform with much harmonic content, well suited to the generation of the "mechanical" sound.

to .-7 volts, and by the time required for the capacitor to charge from ₹.7 volts to +.7 volts. This time is a function of the size of the resistor, the value of the capacitor and the saturation voltage of the op amp, all of which are approximately constant.

Assume now that the control voltage input connected to the cathode of the diode is 5 volts, rather than 0 volts. The operation of the circuit is now altered so that the capacitor must charge from -.7 to +5.7 volts, and vice versa. Since no other factors have changed, the time required to charge and discharge the capacitor has increased, thus decreasing the frequency of oscillation.

The signal at the op amp's output is a rectangular wave with levels of approximately plus or minus 12 volts and moderate rise time. This signal is converted to TTL level, and the rise time improved, by the transistor driven from the op amp's output. The resistor attenuator feeding the transistor protects the emitter-base junction from excessive reverse bias, while the inverter following the transistor still further improves the rise time.

Killer Ship Sound

The killer ship sound channel consists of control logic, a low frequency oscillator for warble control, a ramp generator, a VCO, an analog s switch, and a buffer amplifier. The control logic is fairly complex, due to the requirement for both an "enter" sound and an "exit" sound.

The on/off control signal (pin 14) performs two functions: it enables output from the buffer amplifier, and it starts the ramping of the control voltage. The control voltage (at the 1 microfarad capacitor) is at approximately +9.5 volts before the channel is turned on. This voltage is primarily determined by the 510K and 1 meg resistor voltage divider, working

VECTORBEAM MONITOR OPERATION

The vectorbeam [tm] monitor can be divided into two basic sections. One section is the deflection amplifiers, and the other section is the high voltage and cathode drive circuit.

The deflection amplifier can be further divided into two indentical channels: one for vertical deflection, and one for horizontal deflection. We will describe the operation of only one channel (vertical) and the same theory of operation will also hold true for the horizontal section.

Digital information, in the form of a twelve-bit word, is applied to the input of the DAC-80 digital to analog converter (U101) on pins one through twelve. The most significant bit (MSB) is applied to pin one, and the least significant bit is applied to pin twelve. The DAC-80 makes the necessary c onversion from digital signals to analog signals which are outputted as analog voltage signals on Pin fifteen (which is proportional in level depending on the input word applied). The result is a positive and negative voltage signal about its reference voltage (remember, there is no "sync" signal present, and the signal is not true video as seen in raster scan monitors).

From the DAC-80 the analog signal is then sent to a high-speed analog switch, (U1). The analog switch has two parallel inputs for the display signal, and two controlling inputs which select one of two outputs from the switch. At the outputs is found an R.C. network, which is used to create line length and line position on the screen.

Output fifteen from the switch routes the analog signal through a 5K potentiometer (R102), an 11k resistor, (R103) and to the input of U102 op-amp. The time constant developed by these two resistors and the capacitor (C101) determine the length of the vector line seen on the screen. Adjusting of the potentiometer will adjust the length of the vertical lines seen on the screen.

Output ten from the analog switch routes the signal directly to the input of U102 op-amp, and the resulting time constant of the op-amp input impedence and the capacitor C101 determines the position on the screen of the vector line.

Op Amp, U102, serves a dual purpose: one, it acts as a buffer between the deflection amplifiers and the analog switch; and two, it acts as an "edge gain" amplifier (i.e., height).

At the output of U102, there is a resistor amp, diode network consisting of R105-R110, and CR101 - CR104. This resistor diode network is used to compensate for the non-linear characteristics of the CRT near the edges of the screen. If this circuit were not used, any object displayed on the screen would increase in size as it moved closed to the edges of the screen. Also contained in the circuit is a potentiometer (R109), which adjust the height of the pictures.

From the wiper of R109, the signal proceeds to Q101, which is the first stage of deflection amplification. Q103 is an emitter coupled with Q101 to provide a degenerative feedback loop from the yoke. Q102 is used to provide a constant current source to both emitters.

At this point, the deflection circuit can again be divided into two identical circuits. One circuit, which controls the lower half of the screen, is comprised of Q104, Q106, Q108, and Q110. The other circuit, which controls the upper half of the screen is comprised of Q105, Q107, Q109, and Q111. **

Q104, Q108 and Q110 are three stages of amplification, while Q106 is used as current limiting protection for Q108 and Q110. The same holds true for the other configuration of Q105, Q107, Q109 and Q111. R124 through R129 are used as a current divider network for the yoke.

** In the horizontal section of the deflection amplifier, Q204, Q206, Q208, and Q210 control the left hand side of the screen, and Q205, Q207, Q209, and Q211 control the right hand side of the screen. By dividing the screen in this manner, four quadrants of deflection area have been developed (see vector theory chapter.)

R122, R123, and C102 form a RC network, which compensates for any CEMF that may develop by the expanding and collapsing of the deflection coil's electro-magnetic field.

The high voltage and cathode circuitry is the second section of the monitor. This section also contains the necessary voltage regulation to power the IC's located on the display board as well as develop the high voltage.

U4 and U6 provide plus 15V and minus 15V respectively to power the DAC-80's and the TL081 op-amps on the display board.

U3 and U5 provide plus 18V and minus 18V used in the high voltage transformer (T-1) and oscillator (the oscillator circuit is necessary because there is no horizontal sync. used to develop the high voltage pulses.) The oscillator circuit is comprised of primary windings, Q4 and associated discreet components.

The high voltage 18KV is developed by T1 secondary windings, the high voltage tripler, and the focus circuitry. The potentiometer, R16, is used to adjust the focus of the cathode beam.

One of the secondary windings of T1 develops the necessary cathode voltage, which when measured at the cathode of CR6 should read 88VDC. The cathode circuitry in the vectorbeam ^{tm} monitor is comprised of U7, a 7406 IC used for buffering logic signals which control brightness and blanking. It also contains the transistors, Q1, and Q2, and Q3, and then associated discreet components.

Q1, and the first gate of U7 control the brightness of the cathode signals upon command of the CPU logic board. Q3 and the second gate of U7 control the intensity (blanking) of the cathode signals, also upon command of the CPU board. Q2 is used as a power failure protection for the cathode circuit in the event of a loss of 25V power supply voltage. This protection aids in avoiding phosphor burning on the CRT. R111 is the brightness potentiometer, which adjusts the amplitude of the negative spikes used for brightness and intensification.

TROUBLE SHOOTING HINTS

Read carefully before servicing game. Because of a number of design criteria in your Space Wars game, a problem that arises will generally cause one or both of the twenty five (25) volt fuses or breakers in the power supply to blow. When this occurs, the following procedures will aid in locating the fault assembly. It is important that this procedure be followed in the order in which it is written!

1. Unplug the game and short or meter the two filter capacitors found in the power supply. These are the two 20,000 micro-fared capacitors mounted near the transformer. They will maintain a charge when the fuse(s) are blown.

2. Replace the fuse(s) with MDL-3 Fuses.

3. Disconnect the Molex plug and the ribbon connector from the monitor.

4. Plug in the game again and observe the fuses.

5. If the fuses remain in tact, place a credit on the game.

6. Start a game as if you were going to play, and listen for the game sounds.

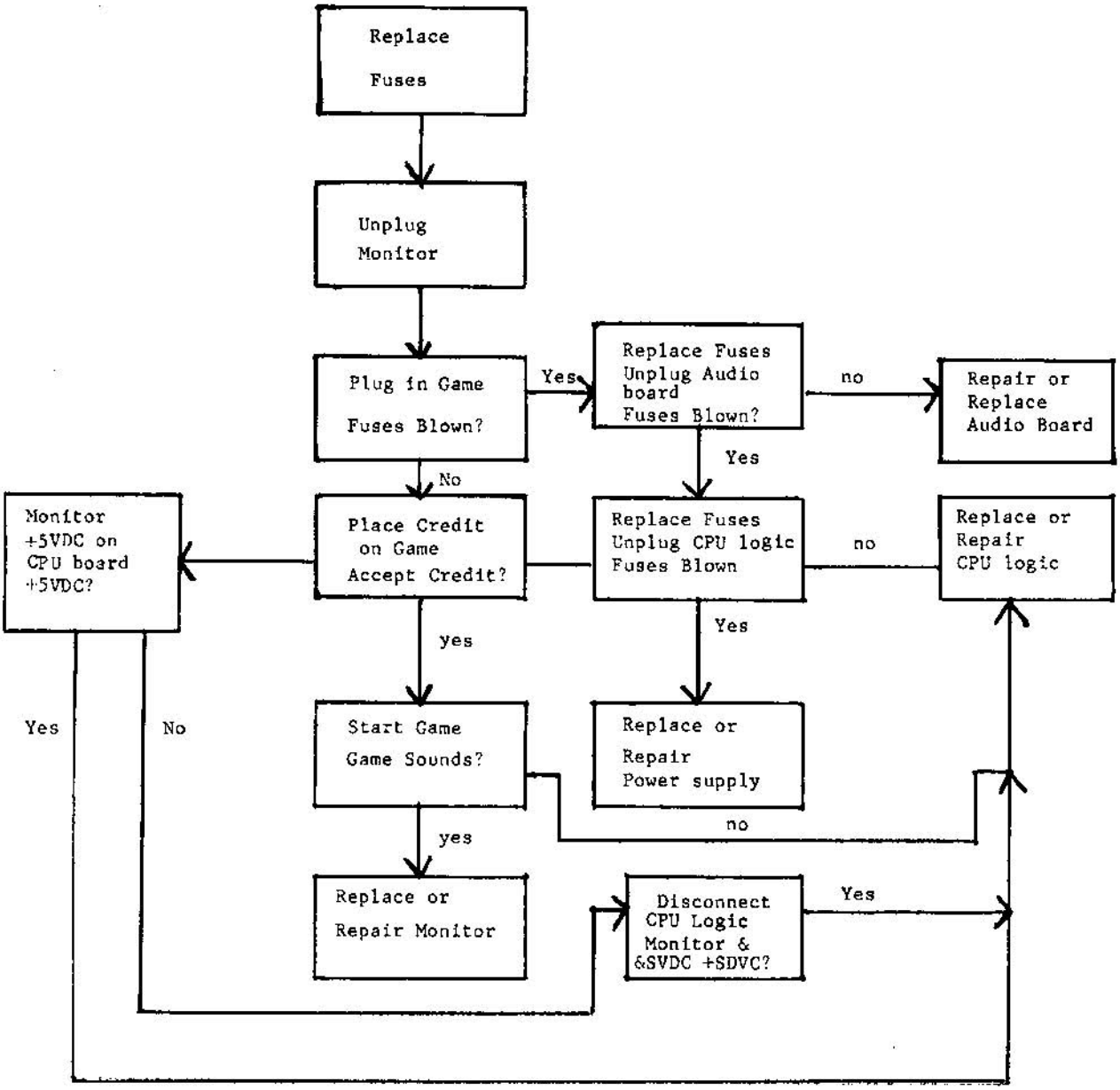
7. If the sounds of the game (acceleration and fire) are present, the problem is in the monitor. If the sounds are not present, or if they are distorted, the problem generally is in the CPU logic board.

The reasoning behind this procedure is that if a failure occurs, in the CPU logic board, it will enter a "constant reset" mode. When the CPU logic board is in this mode of operation, or when there is a lack of computer information at the monitor input (i.e., disconnected a faulty ribbon cable), the monitor will automatically deflect the electron beam off the screen to protect the phosphors in the CRT. When this occurs, the monitor deflection amplifiers will enter a current limiting state and eventually cause the fuses to blow.

For further troubleshooting procedures, use the flow chart provided.

NOTE: It is important to follow steps one and two every time a fuse blows, to protect yourself from electrical shock, and also to protect the game from further damage.

TROUBLE SHOOTING FLOW CHART

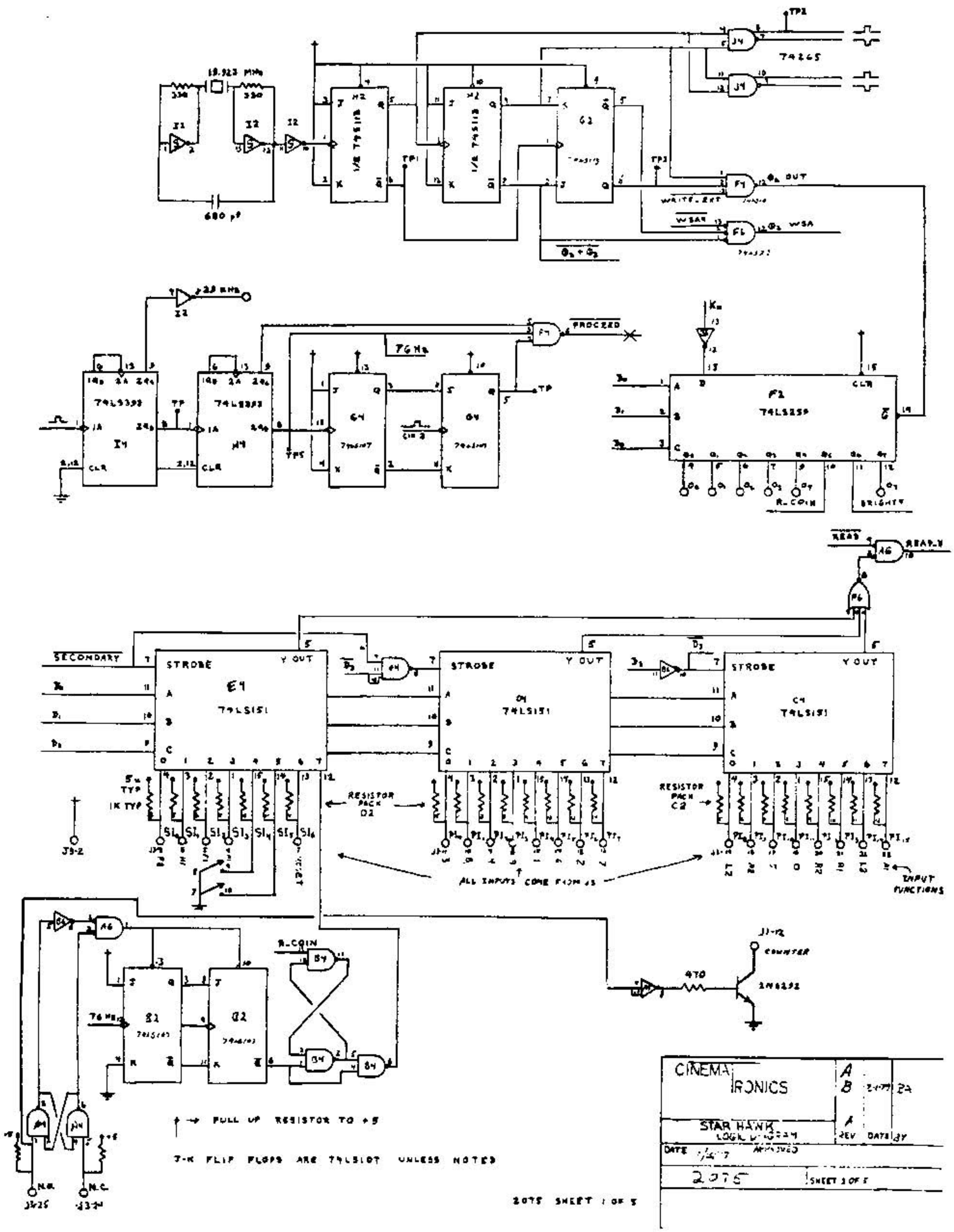


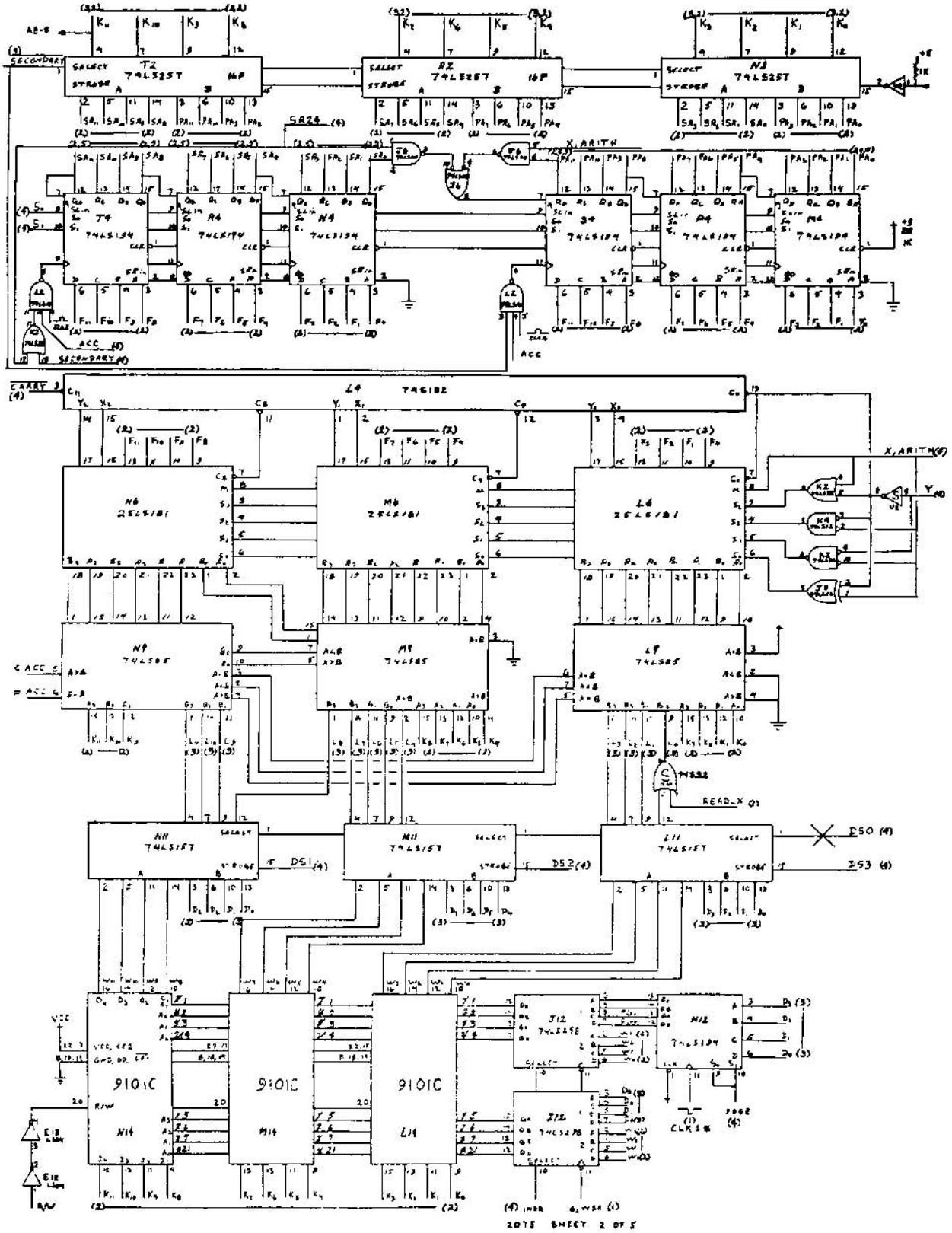
SUGGESTED PARTS FOR STOCK

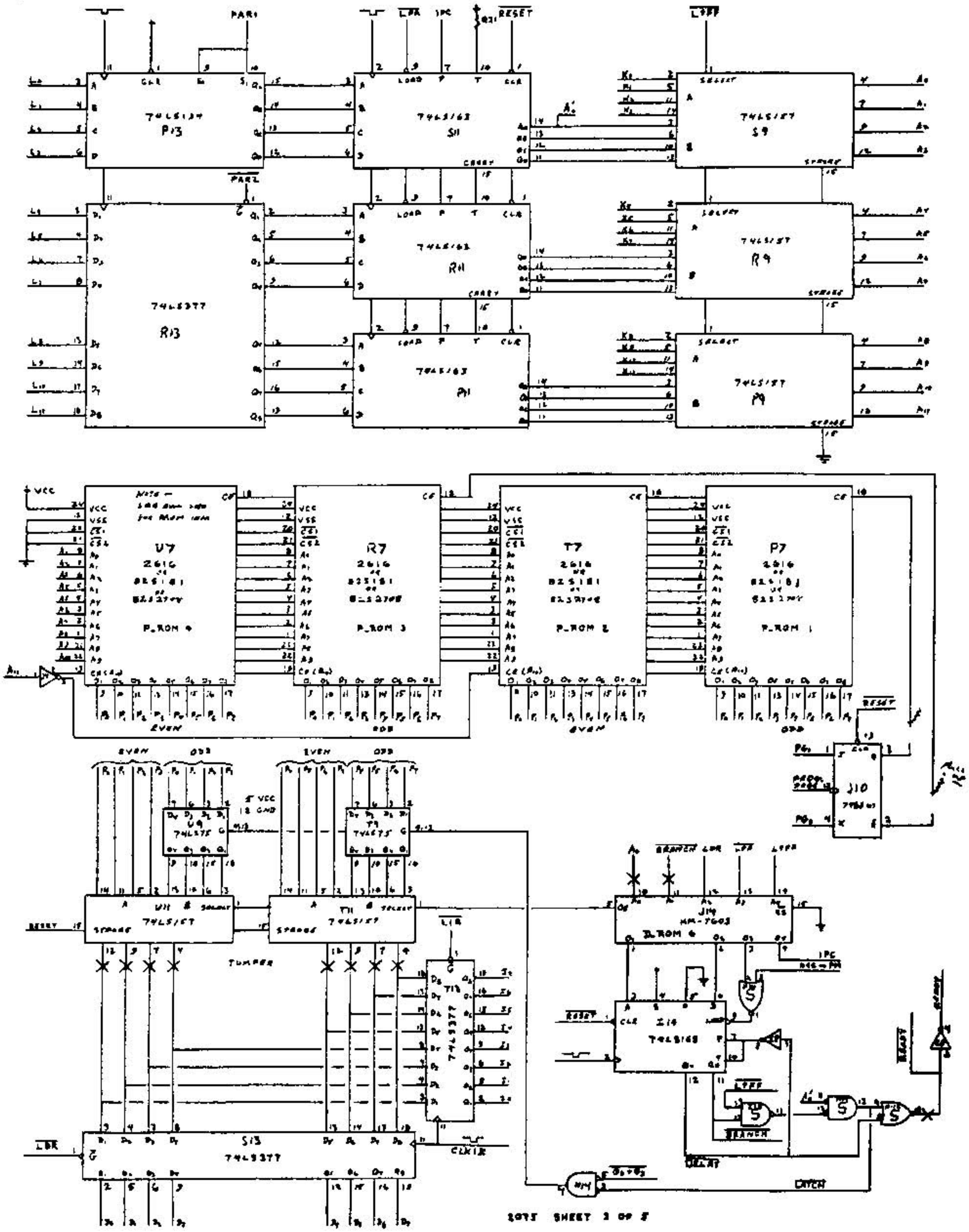
Due to the fact that the vectorbeam [tm] system is a new type of display technology, there are a number of components used which may have limited availability from your local parts suppliers. It is suggested that the following list of parts be purchased from Cinematronics in the event servicing of your game becomes necessary:

1. TL182 - Analog Switch
2. TL081 - Op Amp
3. 7918 - Regulator IC
4. 7915 - Regulator IC
5. 7818 - Regulator IC
6. 7815 - Regulator IC
7. LF 1331D - High speed analog switch
8. DAC-80 Digital to Analog Convertor **
9. 74LS259 - IC (Texas Instruments only)
10. 74LS32 - IC
11. Set D-ROMS (1-6)
12. Masked ROMS

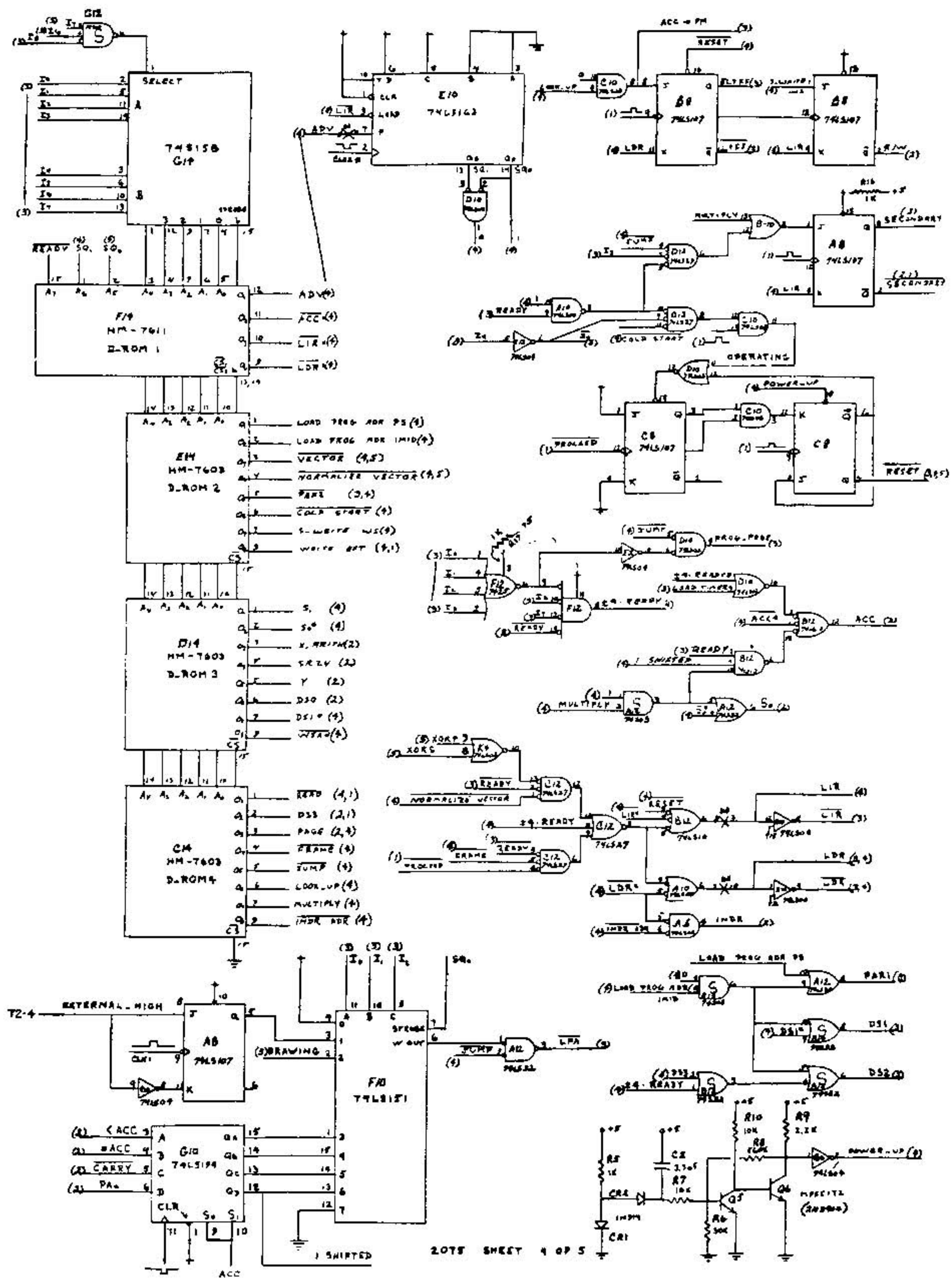
Note: Contact factory for current prices

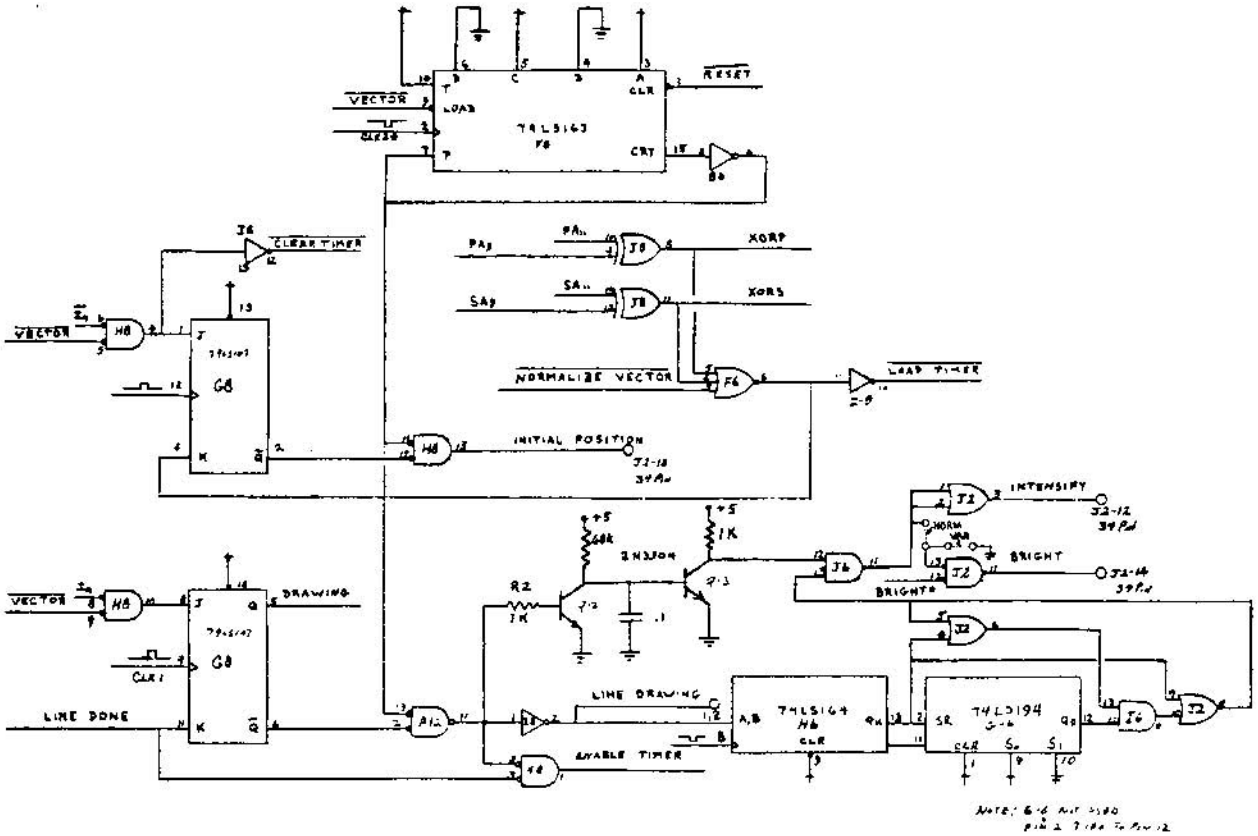

18.923 MHz
680 pF
74265
TP1
TP2
TP3
Φ_1 OUT
WRITE-EXT
WSAR
Φ_2 WSA
$\overline{\Phi_1 + \Phi_2}$
PROCEED
76 KHz
74LS393
74LS259
CLR
R.COIN
BRIGHT
READ
READ-X
SECONDARY
STROBE
Y OUT
E4
74LS151
D4
74LS151
C4
74LS151
RESISTOR PACK D2
RESISTOR PACK C2
5K TYP
1K TYP
ALL INPUTS COME FROM J3
INPUT FUNCTIONS
COUNTER
470
2N6292
N.O.
N.C.
→ PULL UP RESISTOR TO +5
J-K FLIP FLOPS ARE 74LS107 UNLESS NOTED
CINEMATRONICS
STAR HAWK
LOGIC DIAGRAM
REV
DATE
BY
APPROVED
2075
SHEET 1 OF 5
2075 SHEET 1 OF 5

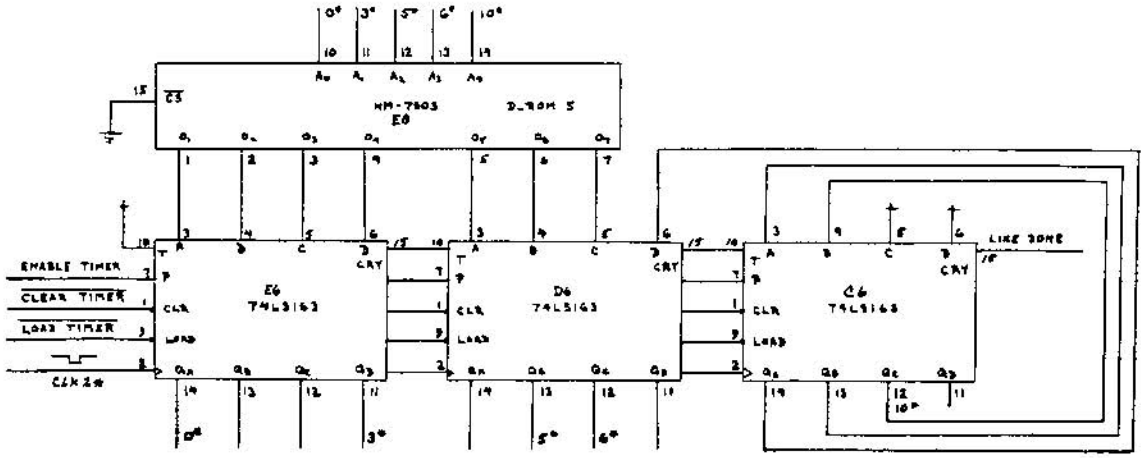


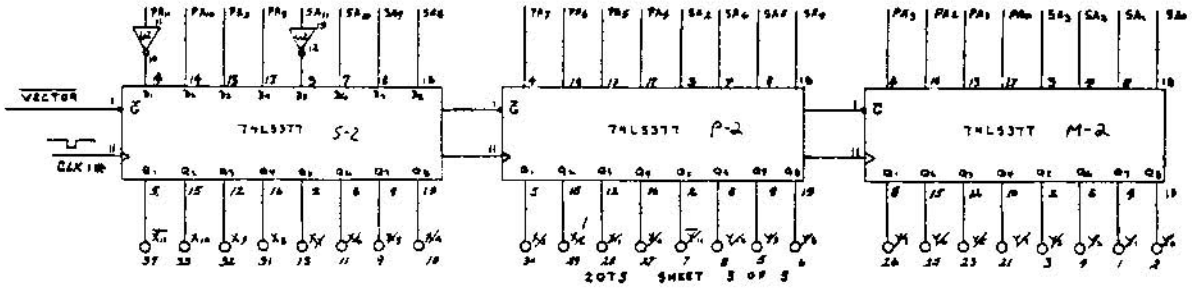


74LS377
R13
P13
74LS163
S11
R11
P11
74LS157
S9
R9
P9
U7
R7
T7
P7
2616
P-ROM 4
P-ROM 3
P-ROM 2
P-ROM 1
EVEN
ODD
RESET
J10
U9
T9
U11
T11
S13
T13
JUMPER
CLK13
J14
I14
74LS163
LATCH
DELAY
BRANCH

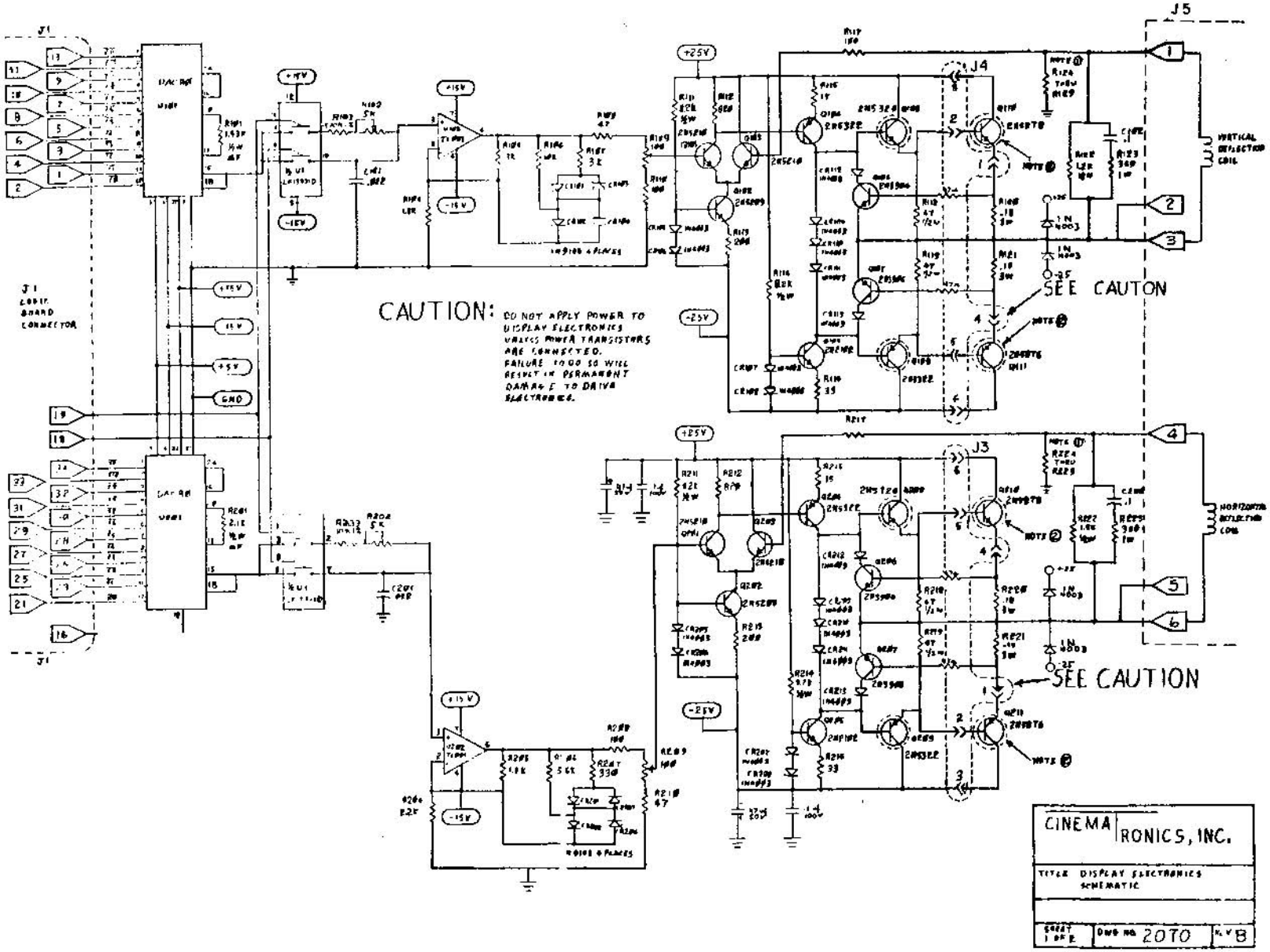

74S158
HM-7611
D-ROM 1
HM-7603
D-ROM 2
D-ROM 3
D-ROM4
74LS163
74LS107
74LS151
74LS194
EXTERNAL HIGH
OPERATING
POWER-UP
LOAD PROG ADR PS
2075 SHEET 4 OF 5

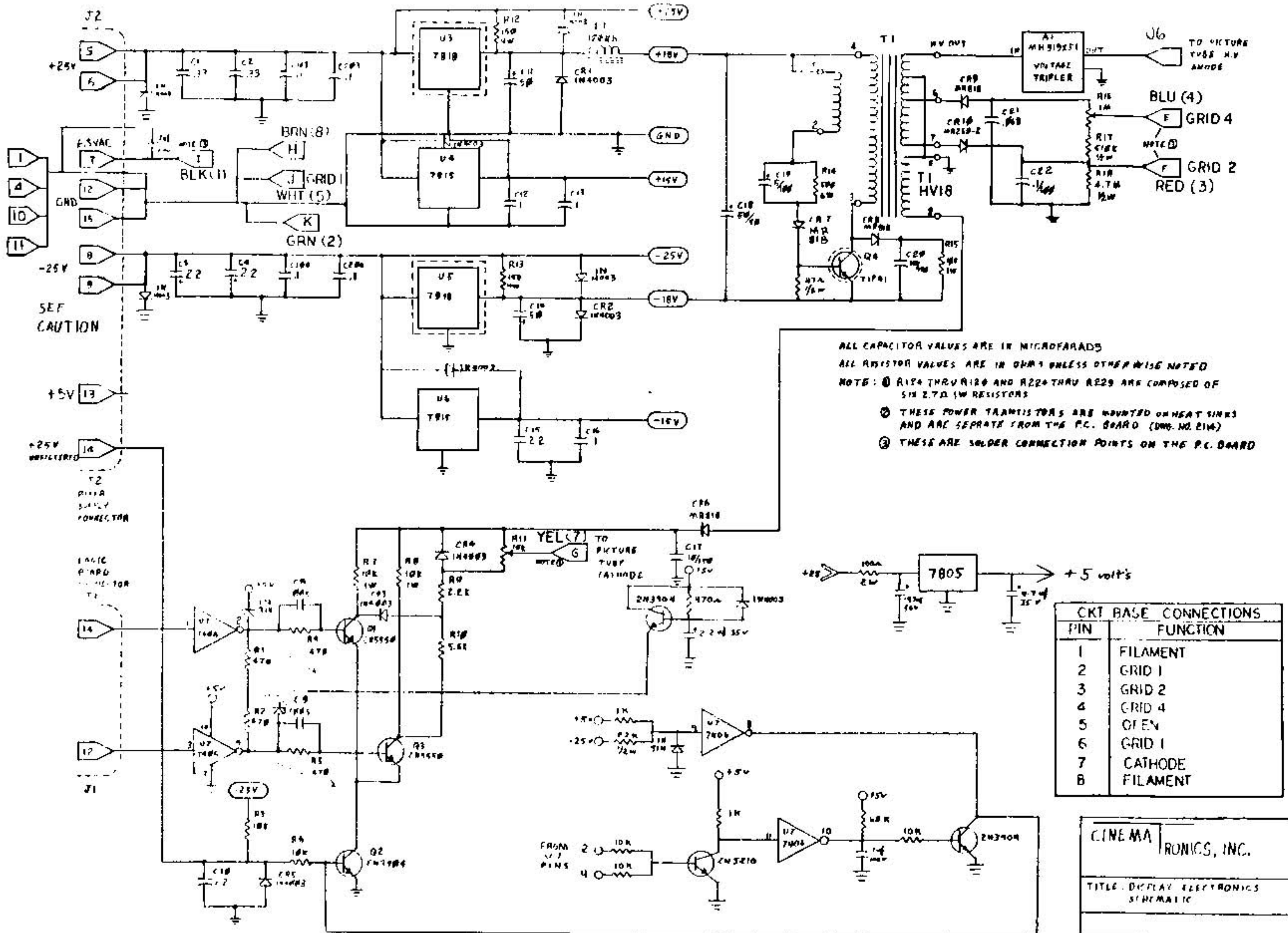






20T5 SHEET 3 OF 5


J5
J4
J3
J1
J1 LOGIC BOARD CONNECTOR
+25V
-25V
+15V
-15V
GND
CAUTION: DO NOT APPLY POWER TO DISPLAY ELECTRONICS UNLESS POWER TRANSISTORS ARE CONNECTED. FAILURE TO DO SO WILL RESULT IN PERMANENT DAMAGE TO DRIVE ELECTRONICS.
SEE CAUTON
SEE CAUTION
VERTICAL DEFLECTION COIL
HORIZONTAL DEFLECTION COIL
CINEMA RONICS, INC.
TITLE DISPLAY ELECTRONICS SCHEMATIC
SHEET 1 OF 1
DWG NO. 2070
REV B

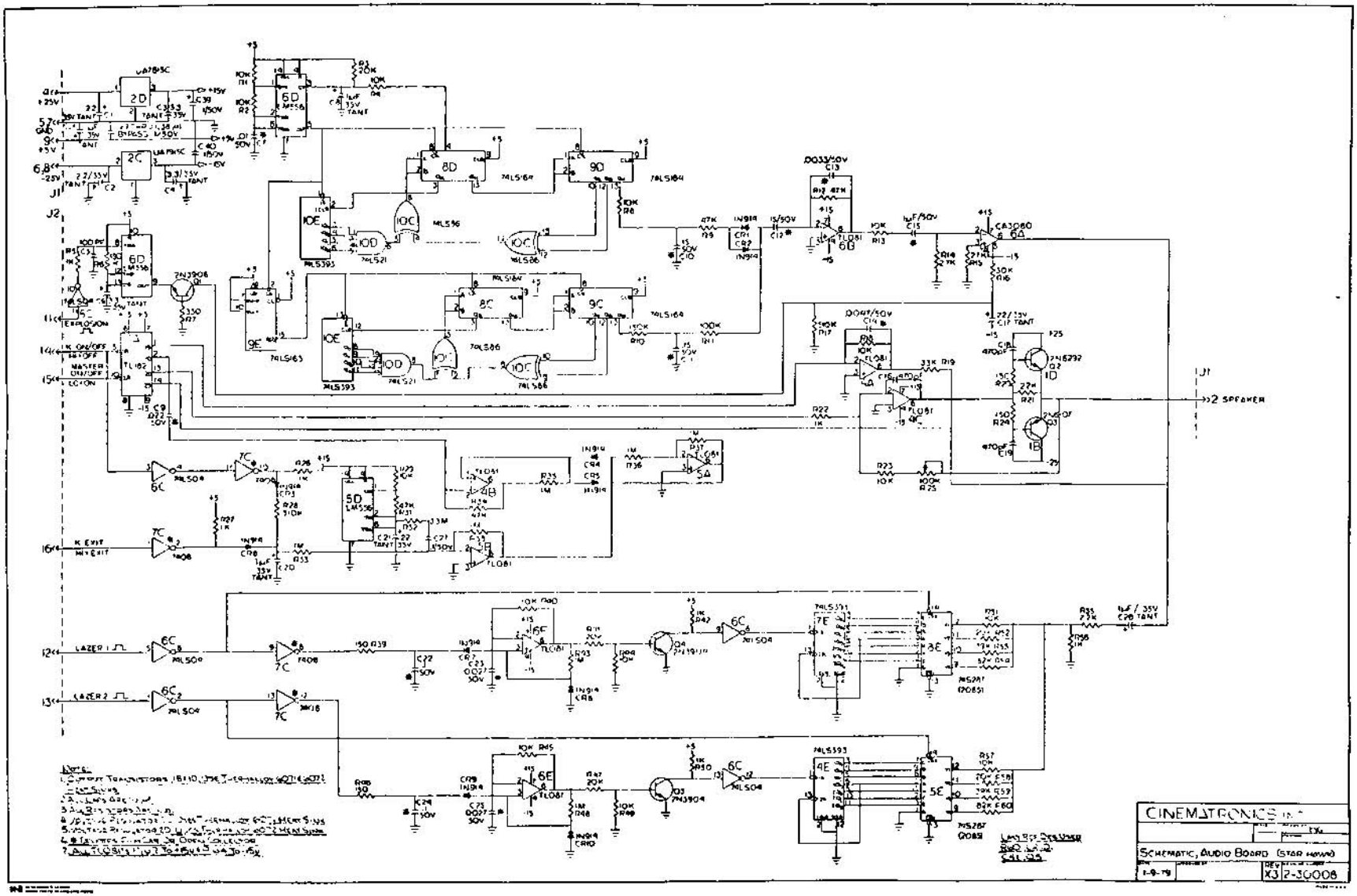


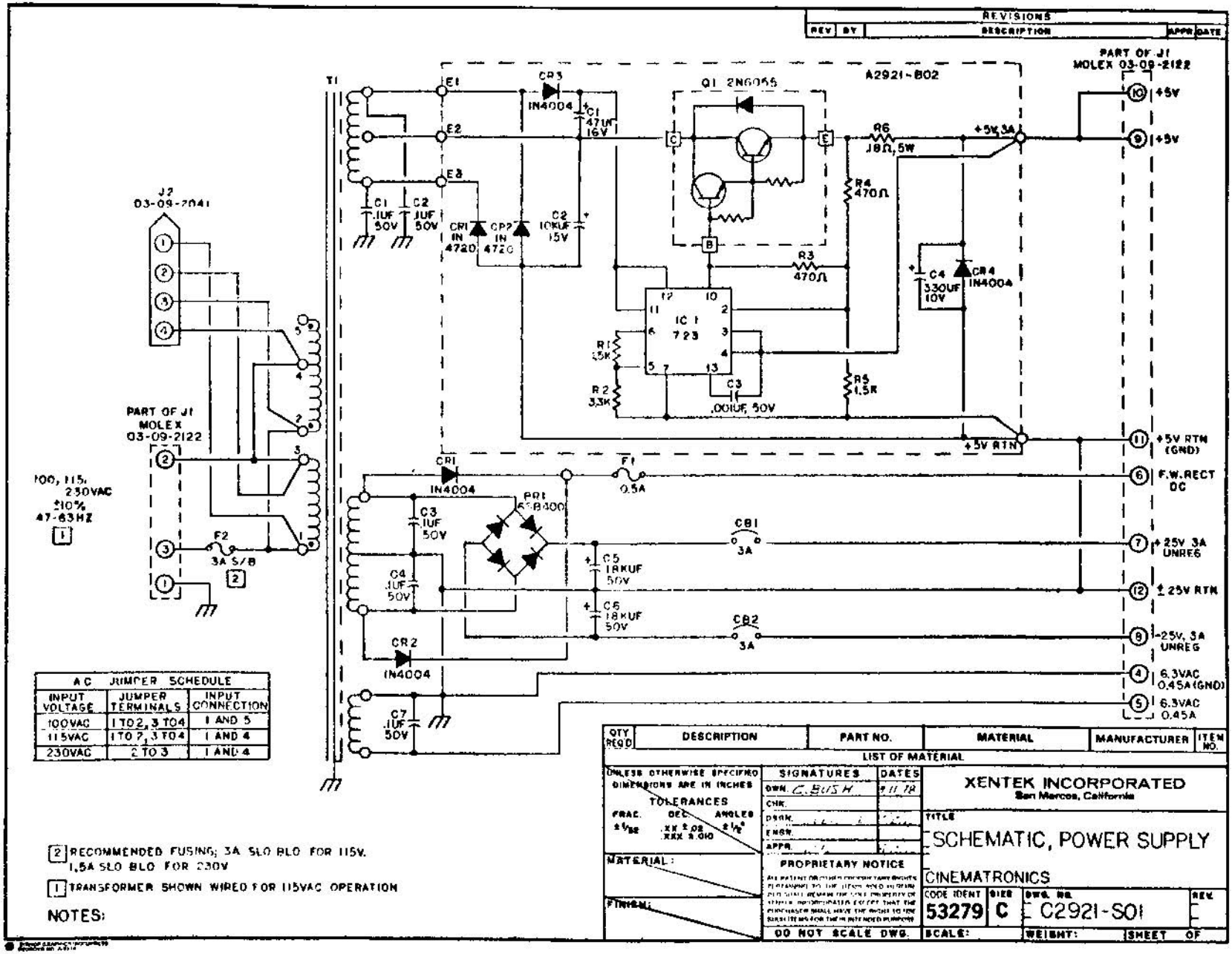
CKT BASE CONNECTIONS	
PIN	FUNCTION
1	FILAMENT
2	GRID 1
3	GRID 2
4	GRID 4
5	OPEN
6	GRID 1
7	CATHODE
8	FILAMENT

CINEMATRONICS, INC.

TITLE: DISPLAY ELECTRONICS SCHEMATIC

SHEET 2 OF 2 | DWG. NO. 2010 | REV. B


CINEMATRONICS
SCHEMATIC, AUDIO BOARD (STAR HAWK)
REV X3
2-30008
J1
TO SPEAKER
LASER 1
LASER 2
ERROR ON
MASTER ON/OFF
K EXIT
MY EXIT


REVISIONS
REV | BY | DESCRIPTION | APPR | DATE
A2921-802
PART OF J1
MOLEX 03-09-2122
J2
03-09-2041
T1
Q1 2N6055
IC 1
723
CR3
IN4004
CR4
IN4004
CR1
IN4004
CR2
IN4004
PART OF J1
MOLEX
03-09-2122
100, 115, 230VAC ±10% 47-63HZ
+5V
+5V
+5V RTN (GND)
F.W. RECT DC
+25V 3A UNREG
±25V RTN
-25V, 3A UNREG
6.3VAC 0.45A (GND)
6.3VAC 0.45A
+5V RTN
AC JUMPER SCHEDULE
INPUT VOLTAGE | JUMPER TERMINALS | INPUT CONNECTION
100VAC | 1 TO 2, 3 TO 4 | 1 AND 5
115VAC | 1 TO 2, 3 TO 4 | 1 AND 4
230VAC | 2 TO 3 | 1 AND 4
[2] RECOMMENDED FUSING; 3A SLO BLO FOR 115V. 1.5A SLO BLO FOR 230V
[1] TRANSFORMER SHOWN WIRED FOR 115VAC OPERATION
NOTES:
QTY REQD | DESCRIPTION | PART NO. | MATERIAL | MANUFACTURER | ITEM NO.
LIST OF MATERIAL
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
FRAC ±1/32 DEC .XX ±.02 .XXX ±.010 ANGLES ±1/2°
MATERIAL:
FINISH:
SIGNATURES | DATES
DWN. C. BUSH | 11 78
CHK.
DSGN.
ENGR.
APPR.
PROPRIETARY NOTICE
DO NOT SCALE DWG.
XENTEK INCORPORATED
San Marcos, California
TITLE
SCHEMATIC, POWER SUPPLY
CINEMATRONICS
CODE IDENT 53279 | SIZE C | DWG. NO. C2921-S01 | REV.
SCALE: | WEIGHT: | SHEET OF