PIONEER LD-V1000

SERVICE MANUAL

Circuit descriptions
Electrical adjustments
Some schematics

2. CIRCUIT DESCRIPTIONS

1. CONT GENERAL

The CONT circuit block diagram is shown in Fig. 1-4.

Z1 is a CPU, and uses Z80 or Z80A series IC, operating with a 2.5 MHz clock signal. Z3 is the memory of the program, and uses an IC2764 (8KBYTE EPROM) to allocate from ADDR 00H to 1FFFH. Z4, as the CPU's working RAM and user's memory, uses 6116 (2KBYTEC-MOSSTATIC RAM) to allocate from ADDR 8000H to 83FFH.

The unit is equipped with two types of I/O, isolated I/O and mapped I/O. Isolated I/O include Z1, Z2, Z7, Z8, Z9, and Z10, while mapped I/O include Z5 and Z6. Each chip is selected by the decoding of the ADDR BUS signal by Z14 (memory select IC). By means of the INSIDE, OUTSIDE, and the REJECT signals, the Z2 (CTC) monitors the player status and the timer function which places an interrupt on the CPU every 1 msec; as the interrupt controller, it generates the INTERRUPT signal, and informs the CPU of the player's status. Z7 and Z8 are parallel ports with specifications identical to PR7820 and PR8020, and their timing chart is shown in Fig. 1-2. Z9 and Z10 are DECODER IC and DISPLAY IC. The DECODER IC has the function of reading the phillips code (24 bit x 3 = 72 bit) contained in 16, 17, and 18H among the NTSC VIDEO signals, and accord with demands from the CPU, outputs these to the CPU. Two lines exist in Z10, and by writing a blank signal, these can be shown so as not to be displayed. Also, the position of the POSITION COUNTER within the DISPLAY can be read.

Z5 and Z6 (IC8255) are used as player control input/output ports. The OSC section which produces the clock for the CPU is made up of Z15, Z18, Z16, and Q1, and produces a 5 MHz foundamental oscillation by means of X1 (X'tal) and Z15. After that output is waveform shaped by Z15, it is frequency divided by Z18 (LS74), and made it 50% duty factor. By using Z16 and Q1, the 2.5 MHz 50% duty factor signal obtained from the output of Z18 is made into an f = 2.5 MHz, V1 = 0V, Vh = Vcc, duty cycle = 50% signal, and in a status fulfilling the Z80 CPU's clock conditions, is output to the CPU and CTC.

The RESET circuit, which uses Z11 (7705), is a reset IC, and is designed so that if the mains voltage falls below rated voltage, the RESET terminal automatically becomes LOW.

The DECODER and DISPLAY IC's (Z9, Z10) are status controlled by the ATN, STB, and TX/RX signals, and the DATA BUS. These signal lines are constructed by the Z21, Z23, Z24, and Z26 gate IC's.

The various signal lines and IC status are shown in the chart below.

CONTROL OF DECODER, DISPLAY IC

	$\overline{ATN}$	$\overline{STB}$	TX/$\overline{RX}$	BUS
DEVICE RESET	0	0	1	
DEVICE SELECT	0	1	1	DEVICE NO.
READ DATA	1	0	0	DATA TO CPU
WRITE DATA	1	0	1	DATA FROM CPU

If the CPU attempts to perform read or write operations with respect to the various devices, but the devices are in a BUSY status, the devices inform the CPU that they are busy, without the ACK switching to LOW.

The circuitry is designed so that in the event that the devices are in the BUSY status, a WAIT is imposed on the CPU by Z18 and Z23. As a result, the CPU is made to wait until the BUSY status is canselled.

A timing chart for ATN, STB, TX/RX, and ACK is shown in the separate Fig. 1-2.

A general outline of the program flow is shown in Fig. 1-3.

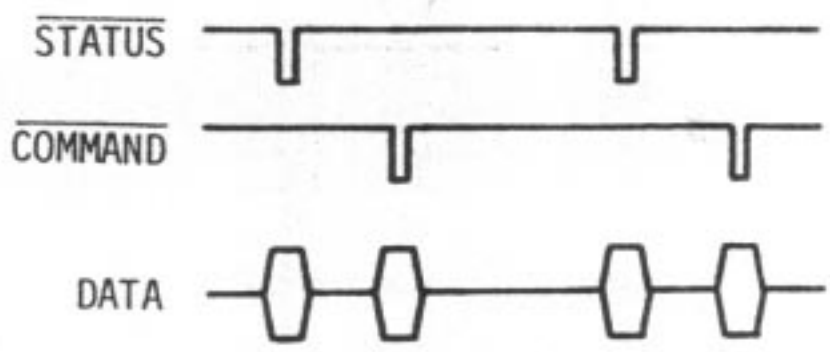


Fig. 1-1 TIMING CHART OF PARALLEL PORT

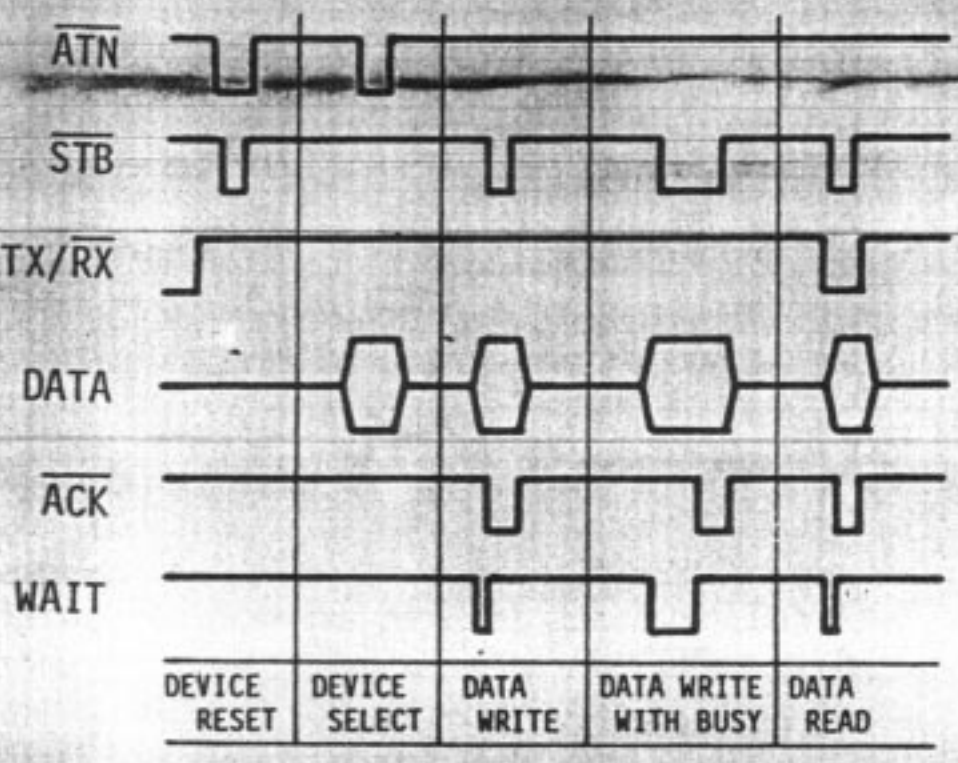


Fig. 1-2 TIMING CHART OF DECODER, DISPLAY IC

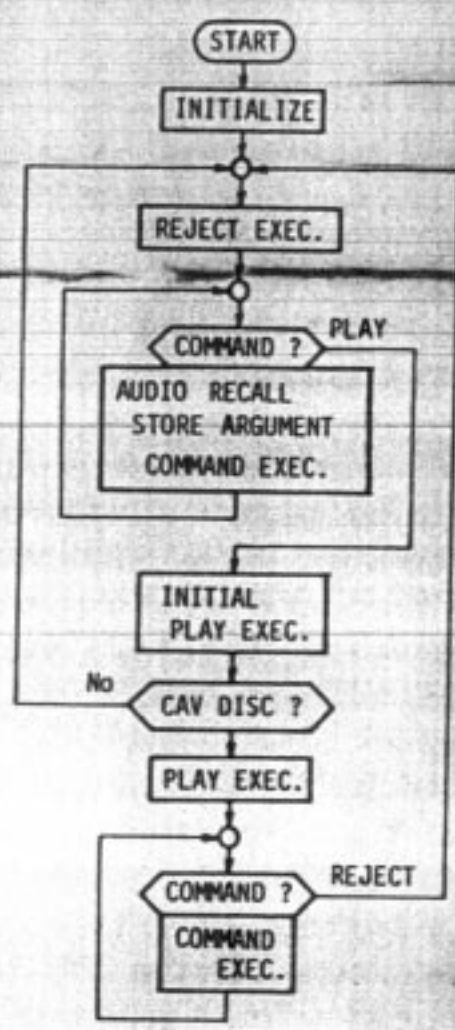


Fig. 1-3 GENERAL FLOW CHART

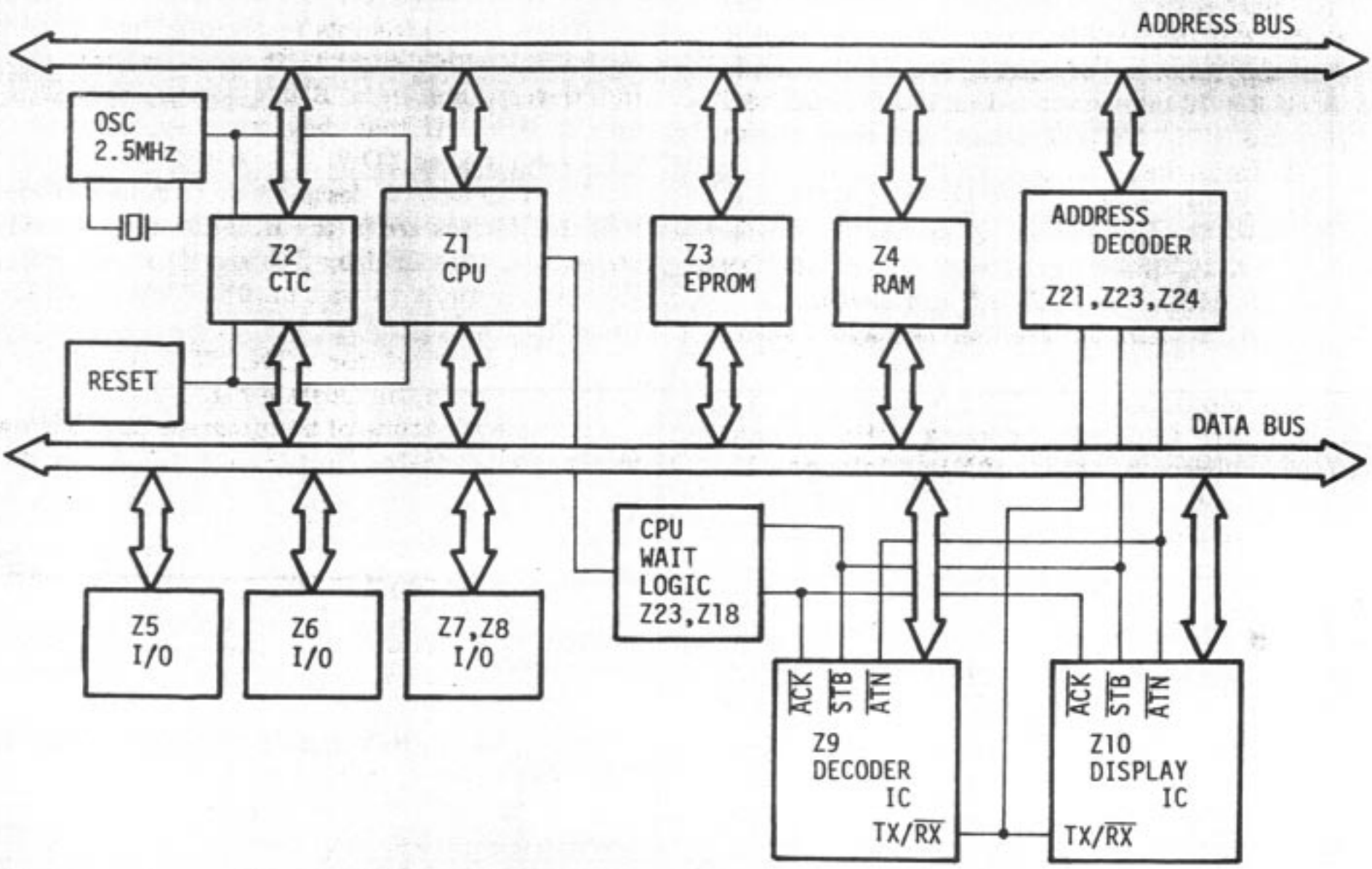


Fig. 1-4 CONT BLOCK DIAGRAM

2. JCAB GENERAL

(1) HIGH-SPEED SEARCH

1-1 Improvement of LOCK IN Ability of TRKG Servo

In order to perform search at high speed, the slider must be made to travel at high speed. TRKG Servo loop condition during the search period was OPEN on the previous 7820 unit, but on the LD-1100, codes were read by a repetitive CLOSE, OPEN operation. However, as the speed of the slider becomes faster, the time the reading beam is focusing on a single track becomes shorter, with the result that the chances of reading the RF signals between data spaces without dropout become smaller.

This fact was an obstacle to attempts to shorten or stabilize the time needed for fast search. In order to solve this problem, search on LD-V1000 with tracking open, sending the slider at high speed, while at the same time, TRKG servo loop (including that of code spacing) is closed at each V-SYNC (1/2 revolution), with the result that the reliability of the data read is increased, making high-speed search possible.

In order to achieve this, it is necessary to stabilize the tracking CLOSE LOCK IN operation, but this is performed by the ON TRACK DETECTOR, which is not present in former players.

1-2 Detection of ON TRACK Signals

The relation between tracks and the 3 beams is shown in Fig. 2-1. As shown in Fig. 2-1, the light reflected from the disc which enters the FOCUS detector (4 divisions), is least when the beam is at the mirror surface between tracks.

On the other hand, the change in the amount of beam spot incident to the 2 tracking detectors, as shown in Fig. 2-1, indicates a mutual inverted phase change. That is because, as shown in Fig. 2-1, the reading beams for the two tracks are arranged so that they are separated by 1/2 cycle of tracking pitch. Accordingly, if the sum of the two is considered, a fixed, direct-current signal corresponding to the average amount of light reflected from the disc can be obtained, regardless of the reading position.

With respect to changes in the power of the beam light and reflectance ratio from the disc, the amount of beam spot incident to the three detectors changes at the same ratio; as a result, for example, by performing an appropriate gain adjustment on the output of the FOCUS detector, a condition like that shown in Fig. 2-1 can be achieved.

When signals have their levels aligned in this way, and are compared by the comparator, a square wave like that shown in the figure is obtained. At LOW level, the fact that the center of the FOCUS beam is above the track can be ascertained from Fig. 2-1.

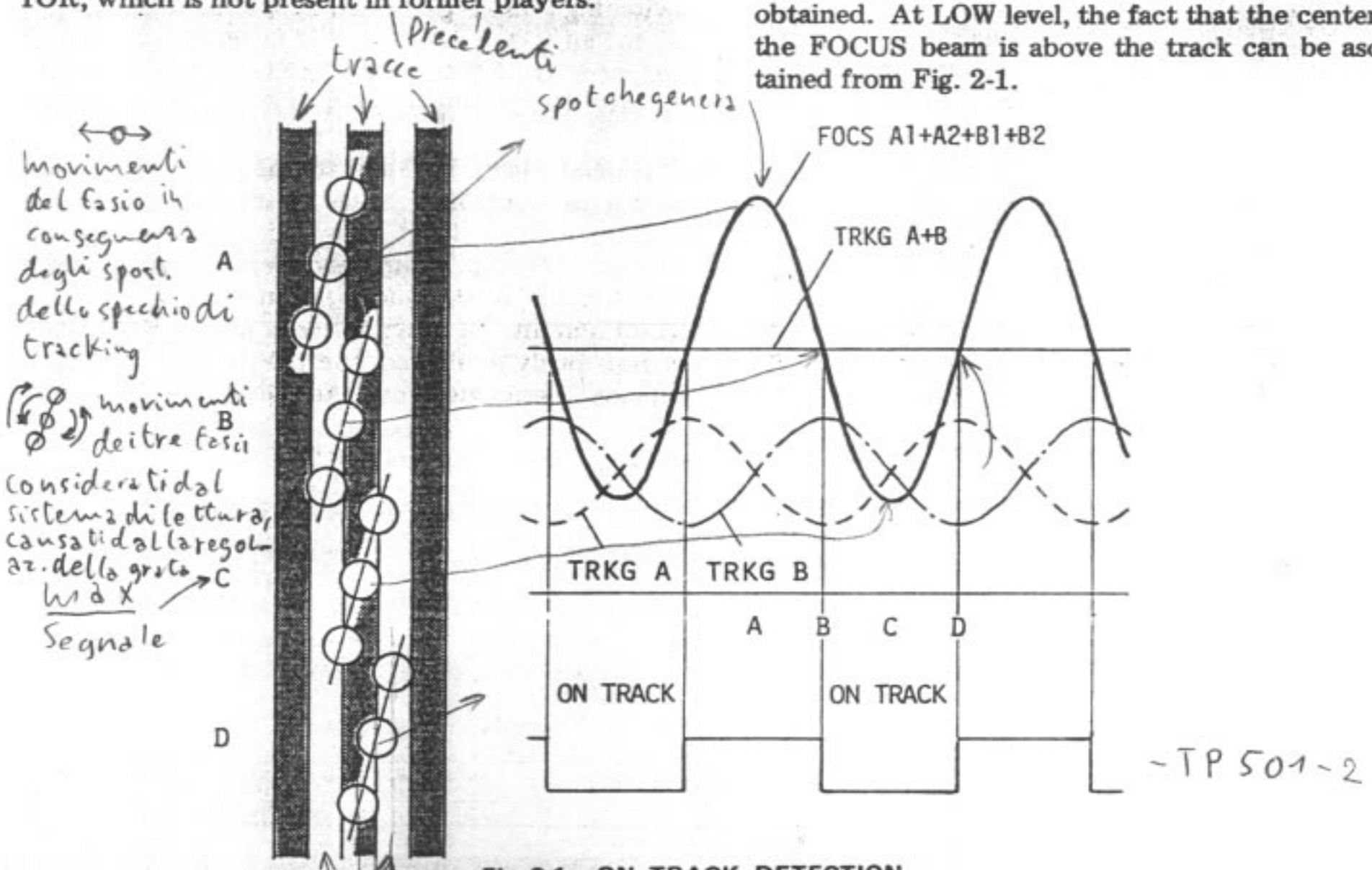


Fig. 2-1 ON TRACK DETECTION

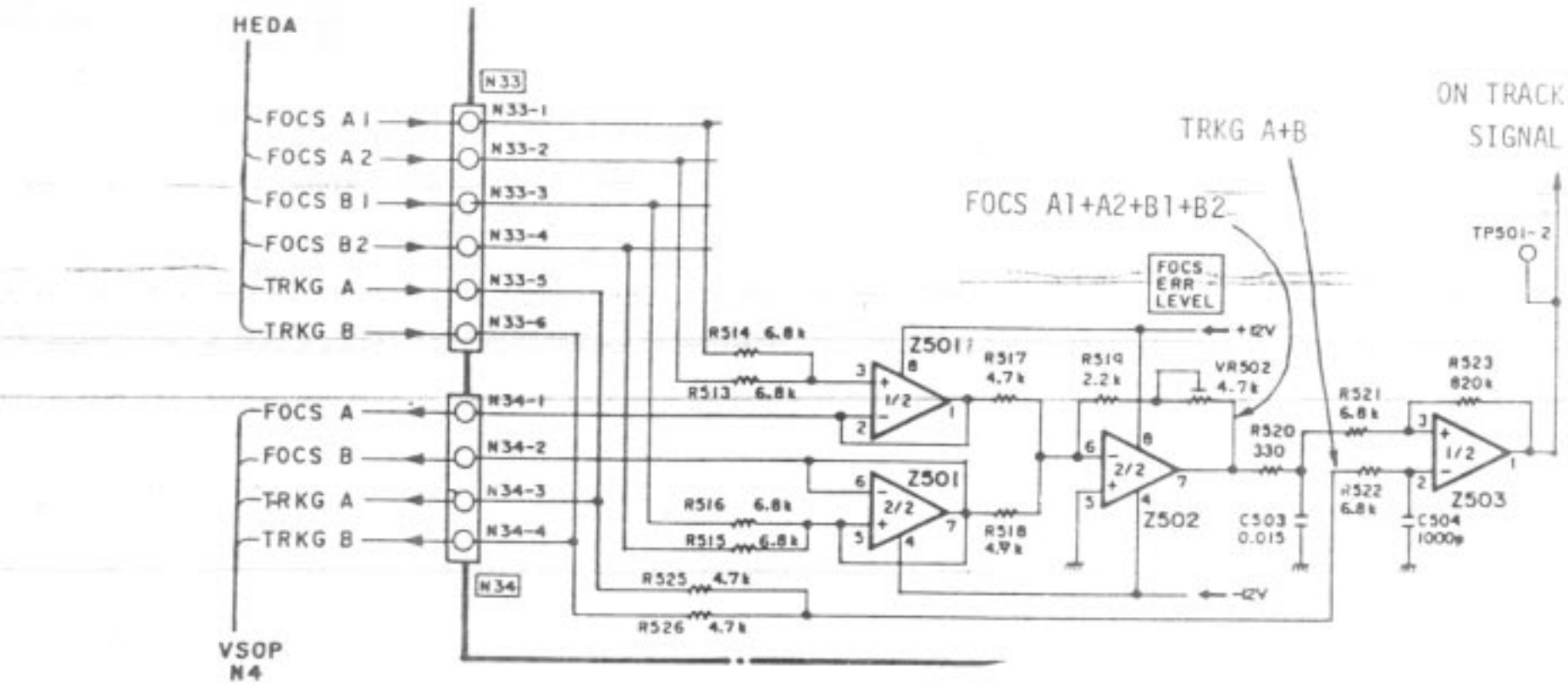


Fig. 2-2 ON TRACK DETECTION CIRCUIT

Fig. 2-2 shows the circuits used in the LD-V1000. This circuitry can be explained as follows: The 4-part FOCS signals input from the RFAM to JCAB are of negative polarity, and TRKG A and B are positive polarity. TRKG A and B are mixed by R525 and R526, pulsive noise is removed by R522 and C504, and the signals are input into the (−) terminal of comparator Z503. On the other hand, of the 4-part FOCS signals, A1, A2 are mixed by R513, R514, coverted to low impedance by Z501-1/2, and sent to the VSOP FOCS SERVO circuit. Then, passing through R519, they are mixed by Z502-1/2 with the identically constructed signals FOCS B1, B2. The output of Z502-1/2 is the total sum of the 4-part signal, and its polarity has also been inverted to positive. Pulsive noise is removed by R520, C503, and the signal is input to the (+) terminal of Z503, where level comparison is performed, and the ON TRACK signal is detected. R521 and R523 add positive feedback to the comparator, generate hysteresis, and give the signal noise-resistance.

1-3 TRKG Servo Equalizer and LOOP SW

Fig. 2-3 shows the TRKG LOOP SW which controls the tracking servo EQ and TRKG MIRROR operation. The TRKG error sent from VSOP is GAIN adjusted by VR503, then, after being phase-advance compensated by Z502-1/2, is input to TRKG LOOP SW Q503, the operation of Q503 is decided by the 3 control inputs which are input after passing through resistors R537, 538, 540. The LOOP OPEN signal, which is sent at TTL level, is made wired OR by the aorementioned 3 resistors; level shift is performed by Q506, and a switching pulse is generated by Q505. Accordingly, when any one of the 3 LOOP OPEN signals becomes H-LEVEL, the TRKG LOOP becomes OPEN. For example, when TRKG OPEN occurs, and Q502 turns ON, centering servo error (to be explained later) is input to the mirror, and the mirror is controlled so as to be fixed near the center of the field of view. In addition, for the purpose of jump, a mirror acceleration pulse passes through the R600, and is input from the MULTI JUMP circuit. In order to close the TRKG LOOP, as previously explained, the LOCK IN operation is quickly performed by the ON TRACK signal. Since the ON TRACK signal is constantly input to R538, if the other 2 LOOP OPEN signals are LOW, the LOCK IN operation occurs.

In this way, this block is the place where the signals controlling mirror movement are selected.

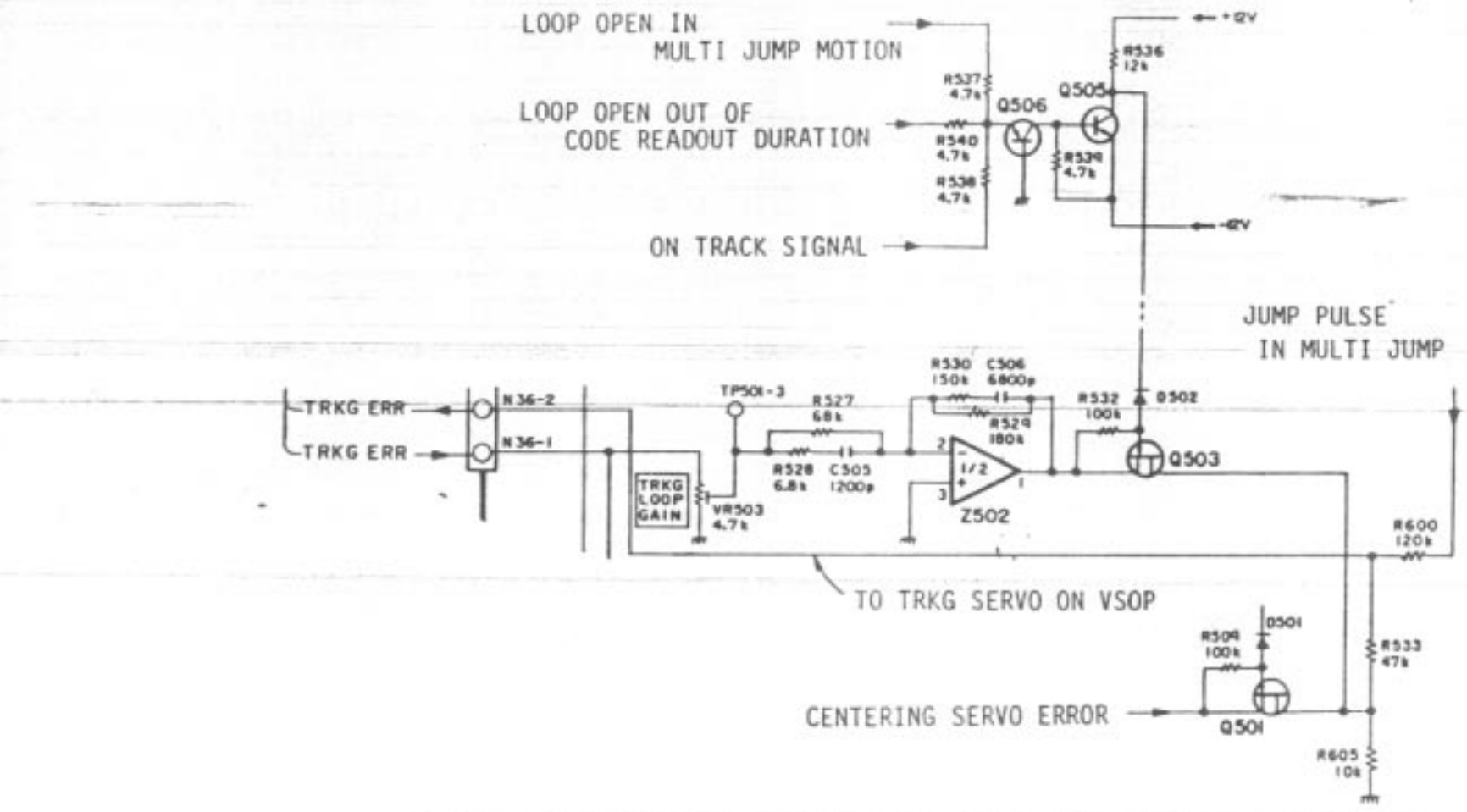


Fig. 2-3 TRKG SERVO EQUALIZER AND LOOP CONTROL CIRCUIT

1-4 Centering Servo

This block is designed so as to prevent the reading beam from deviating toward the outside of the objective lens's field during search, thus causing a loss of good reading operation. As shown in Fig. 2-4, when the reading beam is in the center of the lens field, the laser beam returning to the FOCUS detector is also at the center of the detector. Using this characteristic, by taking the sum and error in a different combination from that at the time of FOCS error detection, the direction and size of the deviation from the center of the returning beam above the detector is detected. This is performed by Z509-1/2, while phase compensation is performed by Z509-2/2. By feedback to the mirror, when Q502 is ON at the time of TRKG LOOP OPEN, the mirror is quickly returned to the vicinity of the center of the field. VR501 is an adjustment VR for the purpose of harmonizing the return point and the center of field.

The arrow shows the direction of movement of returning beam spot at time of tacking mirror oscillation.

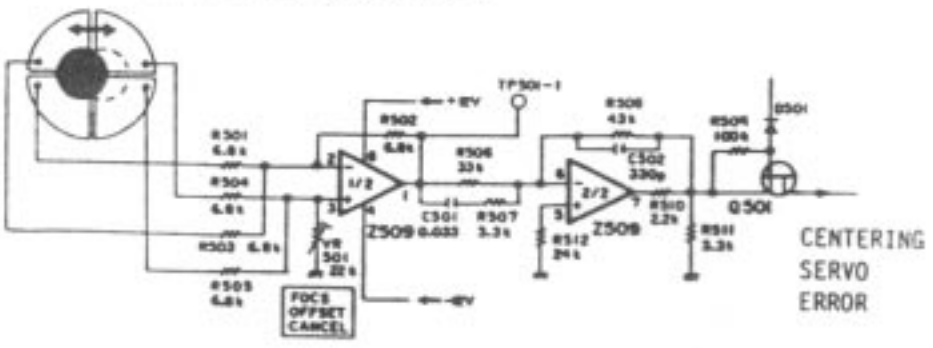


Fig. 2-4 CENTERING SERVO CIRCUIT

1-5 SEARCH CONTROL

This block is the section which generates gate signals for the purpose of CLOSING the TRKG in code readout duration of the vicinity of V-SYNC, and making it OPEN in other duration. However, it also has the function of turning the LOOP SW ON/OFF by the LOOP OPEN signal sent from the VSOP at the time of still, slow, and 3 x speed play mode, and also at the time of the mirror stopper operation.

In addition, it generates the pulse which causes the centering servo to operate, quickly returning the mirror to center following the completion of code reading at time of SEARCH.

The V-SYNC signal is constantly sent from the VSOP, but other than in SEARCH MODE, Z511 is on, with the result that Z504-1/2 is not triggered, and Q511 remains at LOW. However, if a LOOP OPE signal is sent from VSOP at this time, the D505 cathode is grounded, with the result that the current flowing through D506 to the base of Q511 flows to D505, and Q511 becomes HIGH.

This is sent to Q506 in Fig. 2-3, and the TRKG LOOP becomes OPEN.

Since the SCAN MODE becomes LOW level at times of SEARCH, D508 is grounded, and in the same way as the LOOP OPEN from VSOP, Q511 becomes HIGH, and TRKG LOOP becomes OPEN. At the same time, since Z51 becomes OFF (CLEAR), Z504 is triggered at the trailing edge of the V-SYNC, triggerring the next Z504-2/2. This Z504-2/2 pulse generates the gate pulse which becomes HIGH at the playback video signal's

V-SYNC and code duration, with the result that Q511 comes LOW level during this period.

During the period of TRKG OPEN, when Q511 becomes LOW, the fN TRACK signal is constantly input to 538, and R537, R540 are grounded and thus LOCK IN is performed quickly, as explained earlier. Accordingly, in V-SYNC (code duration), TRKG servo is closed, dropout from OFF TRACK is eliminated, and highly reliable code reading is made possible. When Z504-2/2 returns to LOW, Q511 becomes HIGH, and thus for a second time, TRKG LOOP becomes OPEN. However, since the TRKG servo was closed while being moved at high speed, the mirror vibrates toward the outside of the field. As a result, it is necessary to return the mirror to field center again immediately after the transition from CLOSE to OPEN. To this end, Z512 and Q513 generate a gate pulse which turns the centering servo circuit ON. Z512 inverts the output of Z504-2/2, driving the differentiating circuit made up of R555, and C512. In accord differentiating circuit's time constants, Q513 becomes OFF, with the result that Q509 also is OFF.

Accordingly, Q501 becomes ON, and the centering servo operates.

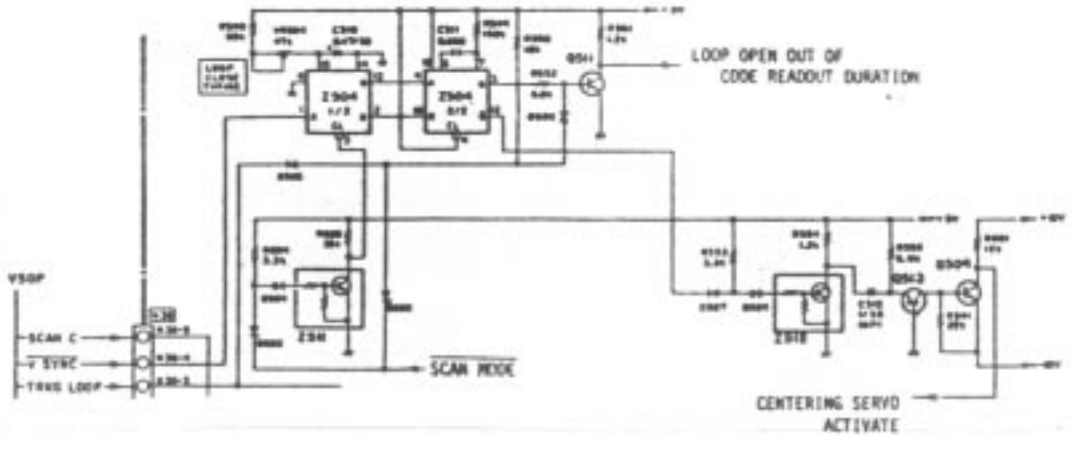


Fig. 2-5 SEARCH CONTROL CIRCUIT

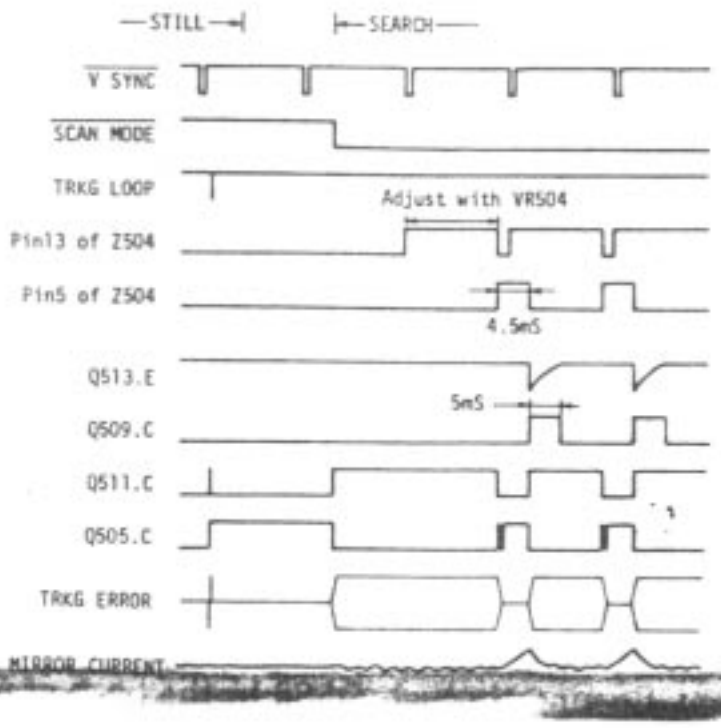


Fig. 2-6 DATA READOUT TIMING CHART

1-6 Timing Circuit

As shown in Fig. 2-8, when the ON TRKG signal is live, during jump control to the adjacent track the LOOP OPEN time of t alone is increased, and the jump becomes unstable.

When TRK LOOP becomes OPEN, at the time of operations of track jump such as still, slow, and X3 jump operation may be disturbed due to the ON TRKG signal. The timing circuit is thus provided so that when TRKG servo is opened at such operations, the ON TRACK signal is kept for a short time at LOW, namely maintained at the level of ON TRACK status (Q508 ON).

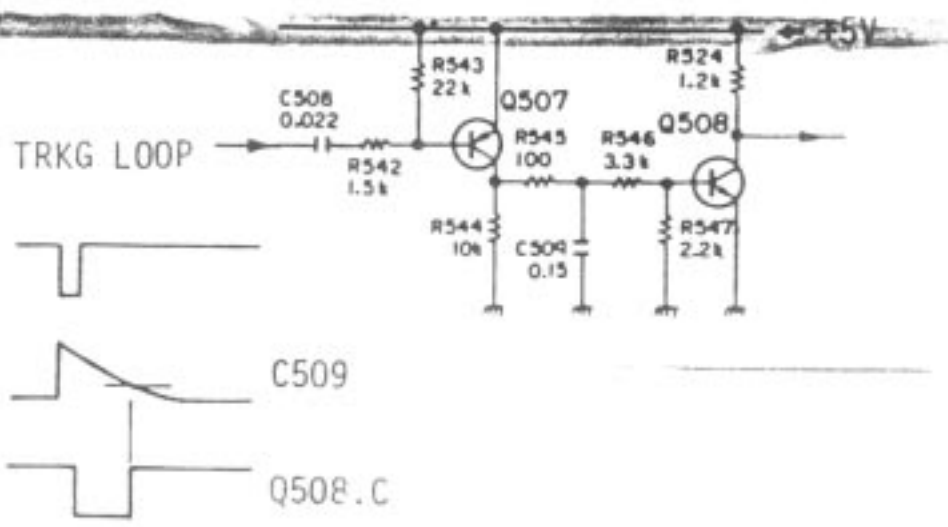


Fig. 2-7 TIMING CIRCUIT

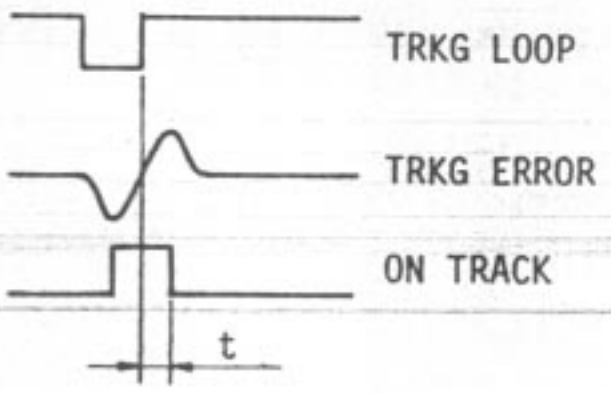


Fig. 2-8 ON TRACK DELAY

(2) MULTI JUMP CIRCUIT

2-1 General

When the MULTI JUMP TRIG is input, the MMV, Z505-1/2 is triggered at its trailing edge, Q514 turns ON, and the input of R537 becomes HIGH, namely, TRKG LOOP OPEN. Also, Q526 turns ON, and acceleration voltage is impressed on the mirror. For example, when jumping to the FWD side, Q517 turns ON, and Q518 turns OFF, so that the voltage input from R616 to Z507-2/2 is impressed on the mirror, and the mirror begins accelerating toward the FWD side. (In the case of REV, the voltage inverted by Z507-1/2 is impressed). The zero crosspoint of the TRKG error signal is detected by Z503, and at its trailing edge, Z505-2/2 triggered, generating a pulse with width of about 8μs. This 8μs pulse becomes the CLOCK PULSE which subtracts the present counter on the CONT board, and is also input to the low pass filter composed of R614 and C513, becoming a negative direct current voltage in accordance with the pulse density. When this is mixed with the reference voltage of the previous R616, the respective polarities are opposed, so they are substracted, and detection is made of how much the relative speed of the reading beam and the track reffers from the reference. If faster than the reference, it is decelerated, and if slower, it is accelerated, so that stable tracking is performed, unaffected by amount of eccentricity, etc.

As the counter is subtracted, when it reaches a remaining 8 tracks, a HIGH level is output as BREAK from the CONT board, and Z513 becomes ON. As a result, the reference voltage supplied by R616 is lowered, the jump speed is correspondingly decreased, making for easy LOCK IN. When the counter becomes zero, JUMP CLR is input, and Z505-1/2 is cleared, Q514 becomes OFF, and TRKG becomes CLOSED.

2-2 Control Circuit for Jump Direction

The FWD/REV signal (TTL level) sent fro CONT is converted to +/- 12V, and a 2-pha control signal is obtained.

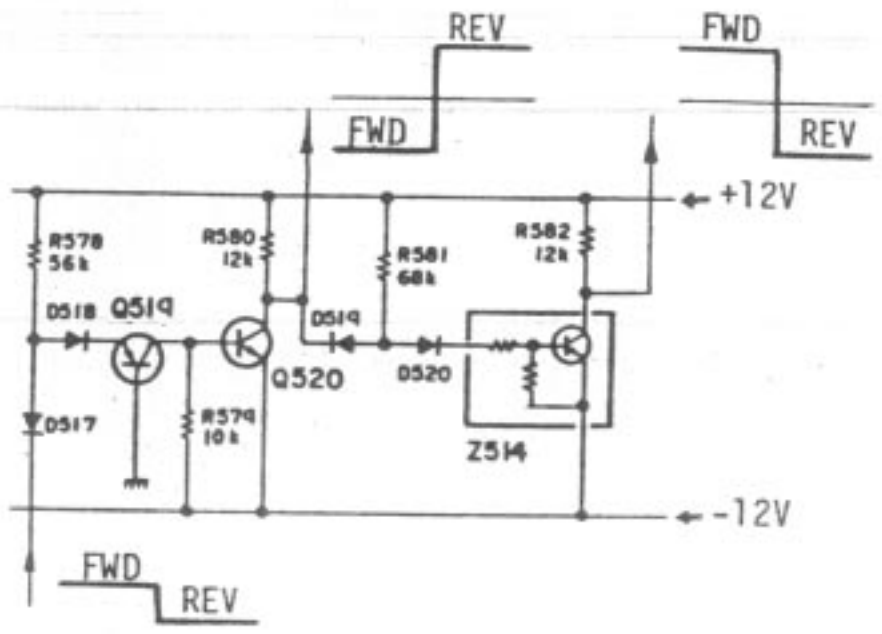


Fig. 2-9 JUMP DIRECTION CONTROL CIRCUIT

2-3 Track Count Pulse Generating Circuit

R602 and C520 are low pass filters for remov ing TRKG error pulsive noise. Since comparato Z503 operates at +5V, D516 is to cut out TRK(error negative polarity portions, -0.6V and belov

The comparator input is inverted depending o which of Q522 and Q523 is ON. Accordingly, th TRKG error waveform and the Z503-2/2 outpu pulse polarity are inverted, but by this, the com parator input is inverted in accord with FWD/RE input signal so that the comparator's output edg polarity is not inverted depending on the directio of the jump, namely depending on whether th reading beam vibrates toward the circumference o toward the outside, and thus the Z505-2/2 i always triggered during off TRKG, regardless o the JUMP direction.

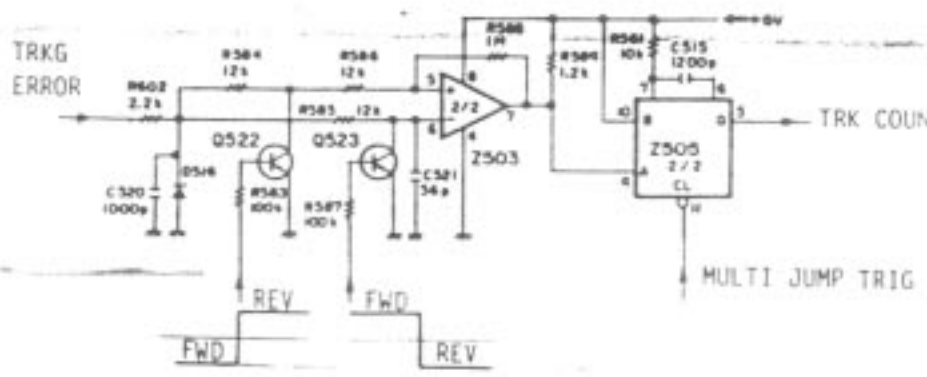


Fig. 2-10 TRACK COUNT PULSE GENERATOR

2-4 JUMP CONTROL Circuit

The operation of this section can be understood from the timing chart in Fig. 2-12, and the contents of 2-1.

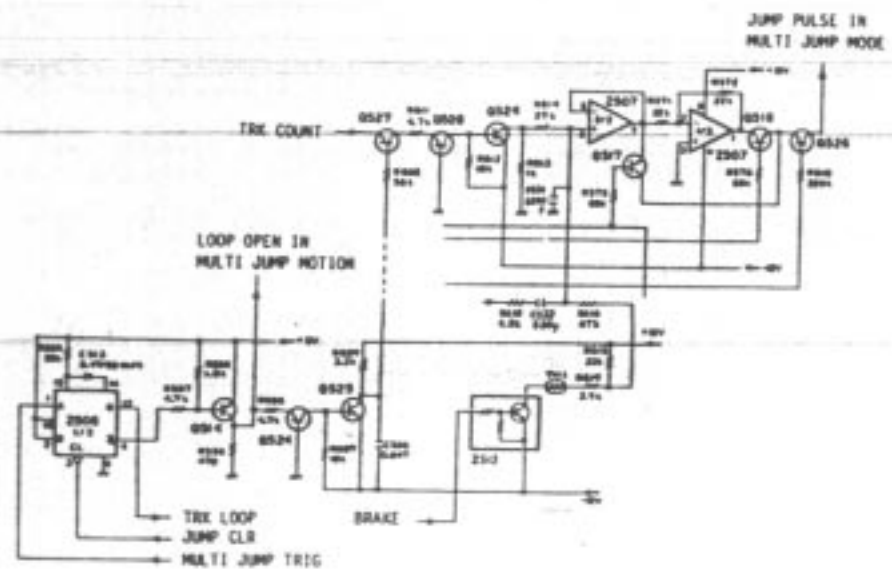


Fig. 2-11 JUMP CONTROL CIRCUIT

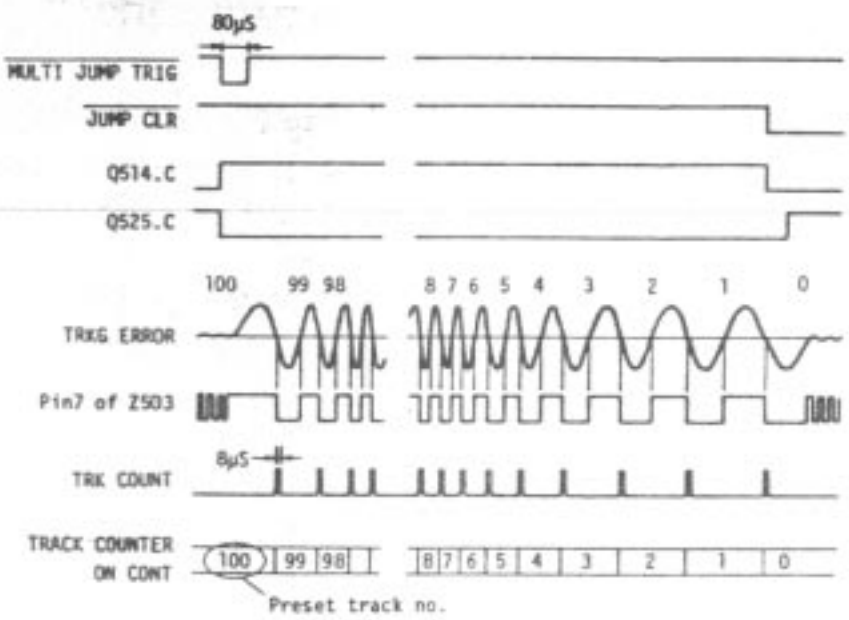


Fig. 2-12 MULTI JUMP TIMING CHART

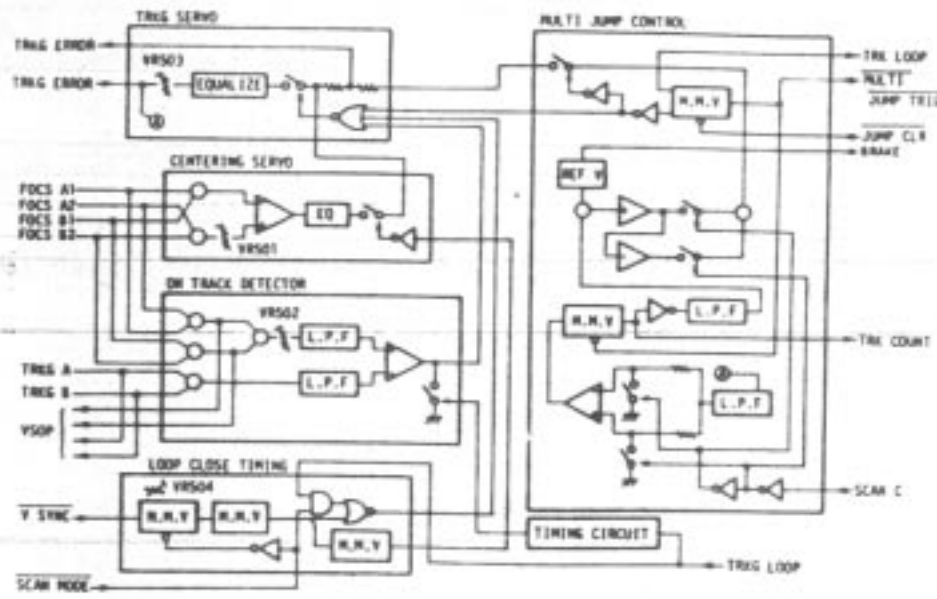


Fig. 2-13 JCAB BLOCK DIAGRAM

3. ELECTRICAL ADJUSTMENTS

PRIOR TO ADJUSTMENT

1. Remove the bottom cover and the screw which fixes the front panel.
2. Remove the five green screws which fix VSOP board to the chassis.
3. Raise the front of the set and hold the set by VSOP board.
4. Open the hood and remove the two screws which fixes the front panel.
5. Disconnect the connector on KEYC board and then remove the front panel.

TP SIGNALS

TP1-1 FOCS error
-2 ~~Test signal input~~ OSC INPUT (FOCS)
-3 FOCS bridge balance
-4 GND
-10 FOCS motor drive

TP2-5 TRKG error
-6 Test signal input
-7 TRKG mirror current (TRKG RETURN)
-8 TRKG loop switch
-9 GND
-11 RF
-12 TANG mirror current (TANG RETURN)

TP3-1 TANG loop switch
-2 PB H
-3 REF H
-4 TANG error
-5 not used
-6 not used (FG)

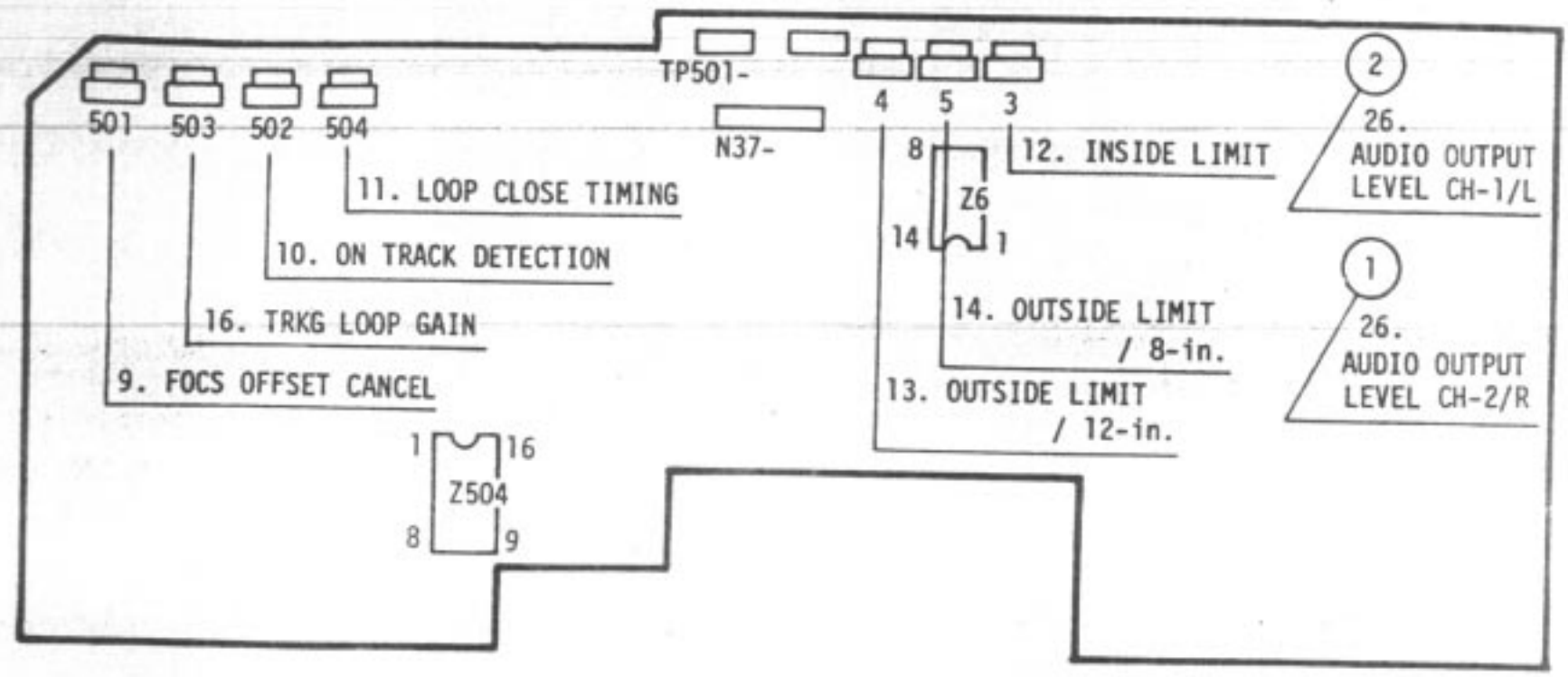
TP501-1 CENTERING SERVO ERROR
2 ON TRACK SIGNAL
3 OSC INPUT

EQUIPMENTS AND TOOLS

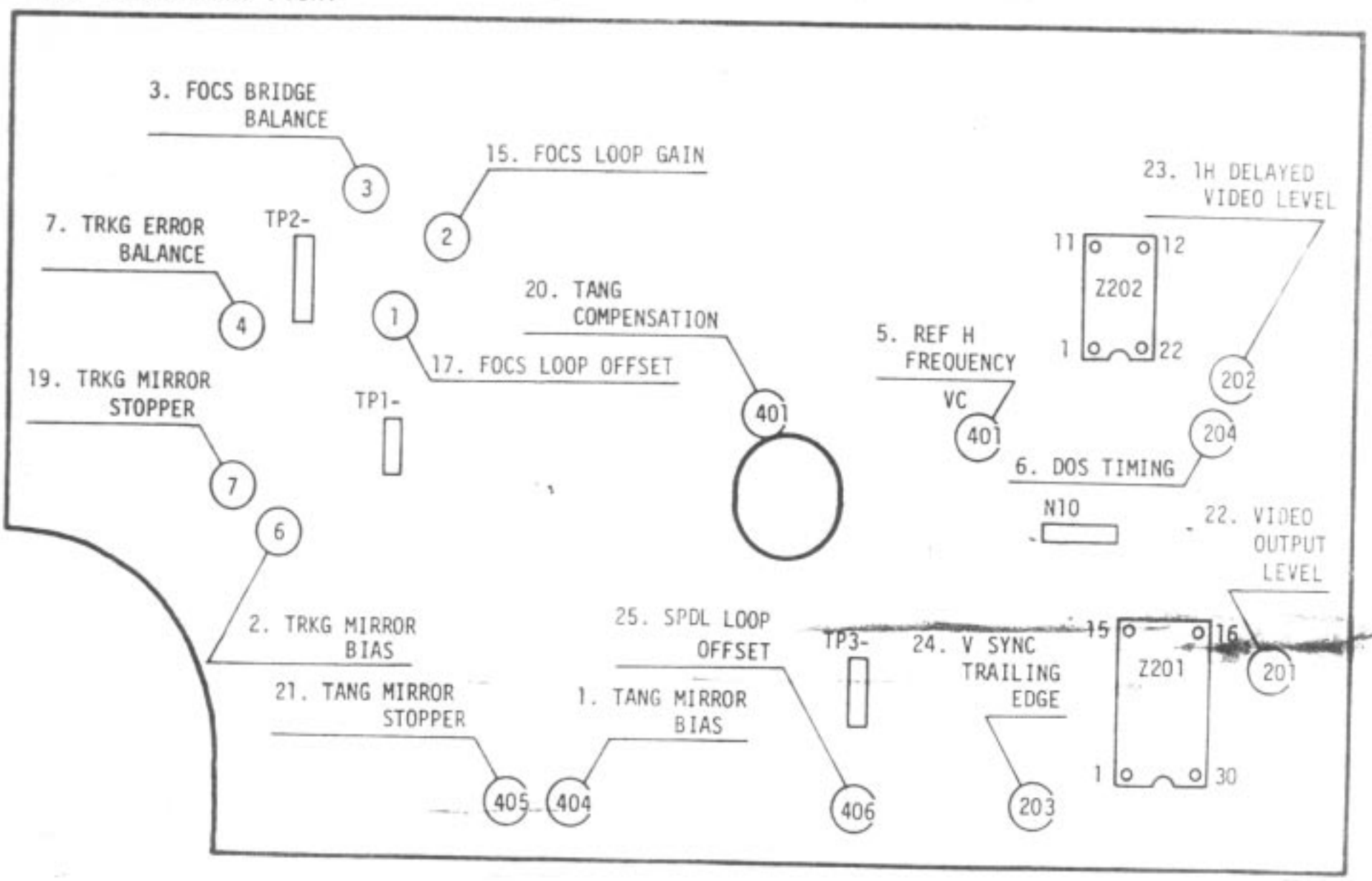
Oscilloscope
Colour TV monitor
Oscillator
Test disc B1
Grating adjustment driver
NTSC video signal generator etc.

WARNING:
EXTREME CARE MUST BE EXERCISED TO LSPS BOARD WHILE WORKING WITH THE PLAYER TO PREVENT POSSIBILITY OF EXPOSING YOURSELF TO DANGEROUS VOLTAGES.

JCAB ADJUSTMENT POINT

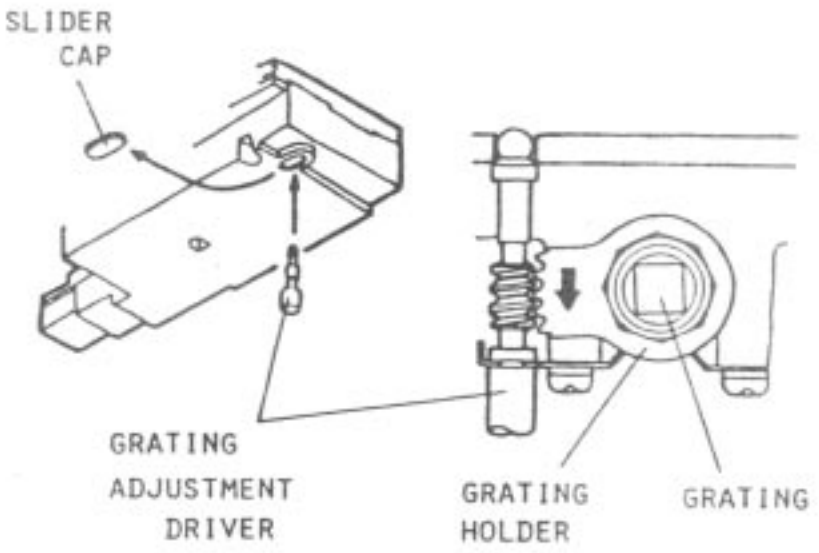


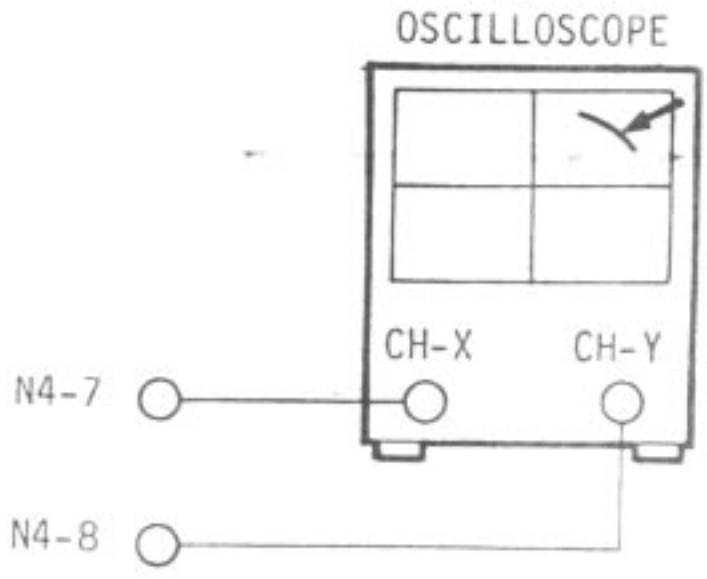
VSOP ADJUSTMENT POINT



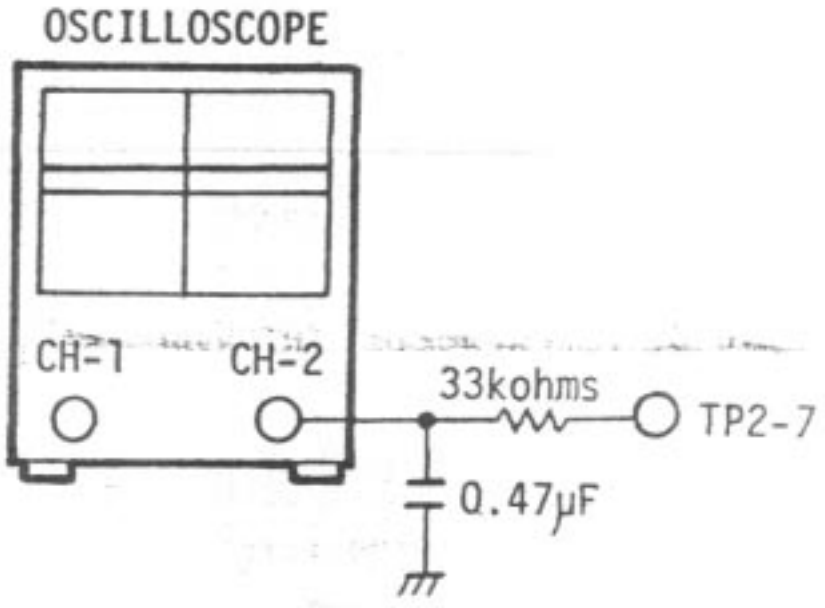
STEP NO.	MODE	SERVO LOOP	CHECK POINT	ADJUST. POINT	DETAIL
1 STP 0	Set up ch 1	–	TP2-12	VR404	**TANG MIRROR BIAS/VSOP** Make sure that a voltage at TP2-12 is 0±20 mV. If not, adjust VR404 to satisfy the before-mentioned standard.
2 STP 1	Set up ch 2	–	TP1-3	VR3	**FOCS BRIDGE BALANCE/VSOP** Connect TP1-10 to GND. Measure a voltage at TP1-3 (an offset voltage of Z2), then disconnect TP1-10 from GND. Adjust VR3 so that a voltage at TP1-3 is 20 mV lower than that measured voltage. This step must be finished within one minute after the power is turned on.
3 STP 1	Set up ch 1	–	TP1-1	VR1	**FOCS OFFSET INITIAL SET/VSOP** Make sure that a voltage at TP1-1 is 0±20 mV. If not, adjust VR1 to satisfy the before-mentioned standard.
4	Set up	–	TP3-3	VC401	**REF. H FREQUENCY/VSOP** Connect CH1 input of the scope to an H-SYNC OUT terminal of an NTSC video generator, and connect CH2 input to TP3-3. With triggering by CH1, adjust VC401 to stop a current of the square waves in CH2. In other way, connect a frequency counter to TP3-3, and adjust VC401 so that the frequency comes 15734 Hz.
5	Set up	–	pin 14 of Z201	VR204	**DOS TIMING/VSOP** Connect a 12th post of [illegible] (LASER ON) to GND. Connect an oscillator output to TP2-11, and input a signal of 5.5 MHz (200 mVp-p). Rotate VR204 fully CW, then back to CCW until a voltage at pin 14 of Z201 turns H to L. Disconnect a 12th post of [illegible] from GND.

STEP NO.	MODE	SERVO LOOP	CHECK POINT	ADJUST. POINT	DETAIL
6 STP 2/3	Still ch 1	TRKG: O/L TANG: O/L	TP2-5	Grating	**TRKG ERROR CHECK/VSOP** Connect TP2-8 and TP3-1 to GND. (TRKG and TANG servo loops are opened.) Make sure that TRKG error level is more than 2Vp-p. If not, a mounted angle of a diffraction grating should be adjusted. Scan to the point where displayed Frame no. comes 14,000 nearby, and then push STOP key on the control jig. Remove a slider cap, and insert a grating driver into the opening. Engage the cogs of the grating holder and the driver. While observing TRKG error, adjust the grating angle to find the smooth null point of the waveform. Then rotate the grating holder in the direction of the arrow to find the first point where maximum TRKG error with smooth envelope is obtained. Set the scope into X-Y mode. Connect CH-X input to N4-7 and CH-Y to N4-8. Adjust the angle finely so that the waveform comes as illustrated.

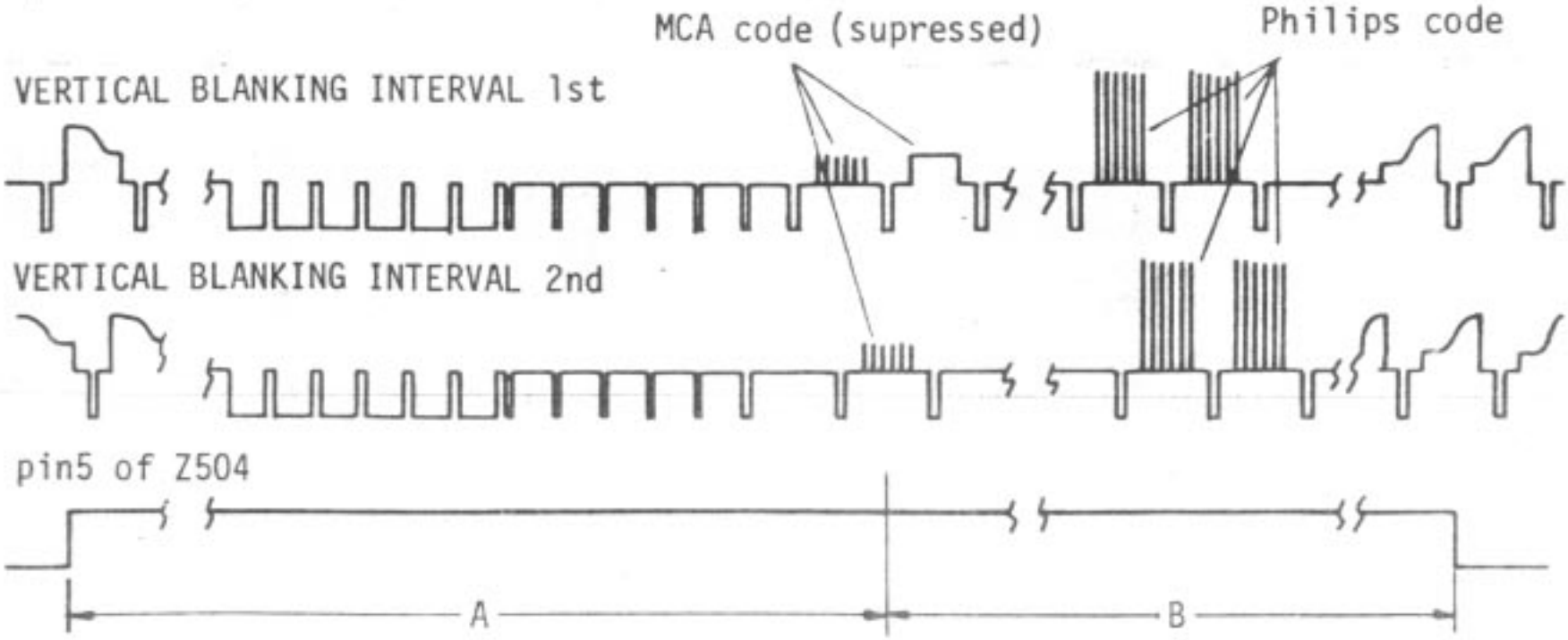




STEP NO.	MODE	SERVO LOOP	CHECK POINT	ADJUST. POINT	DETAIL
7 STP 0	Play ch 2	TRKG: O/L TANG: O/L	TP2-7	VR6	**TRKG MIRROR BIAS/VSOP** Make sure that a voltage at TP2-7 is 0±5 mV. If not, adjust VR6 to satisfy the before-mentioned standard. In this step, use a 1:1 probe and an oscilloscope which is calibrated accurately.
8 STP 2/3	Play ch 1	TRKG: O/L TANG: O/L	TP2-5	VR4	**TRKG ERROR BALANCE/VSOP** Push PLAY key on the control jig and scan to the middle of the disc. Adjust VR4 to where TRKG error waveform is centered on DC 0V.
9 STP 2	Play ch 2	TRKG: O/L TANG: O/L	TP501-1	VR501	**FOCS OFFSET CANCEL/JCAB** Adjust VR501 so that the waveform at TP501-1 is centered on DC 0V.
10	Play	TRKG: O/L TANG: O/L	TP501-2	VR502	**ON TRACK DETECTION/JCAB** Adjust the V position of the scope so that GND level is equal to the center line of the holizontal scale on CRT, and set the input mode of the scope to AC. Adjust VR502 so that the waveform at TP501-2 is centered on the center line on CRT. (The duty cicle of the waveform comes 50%.)

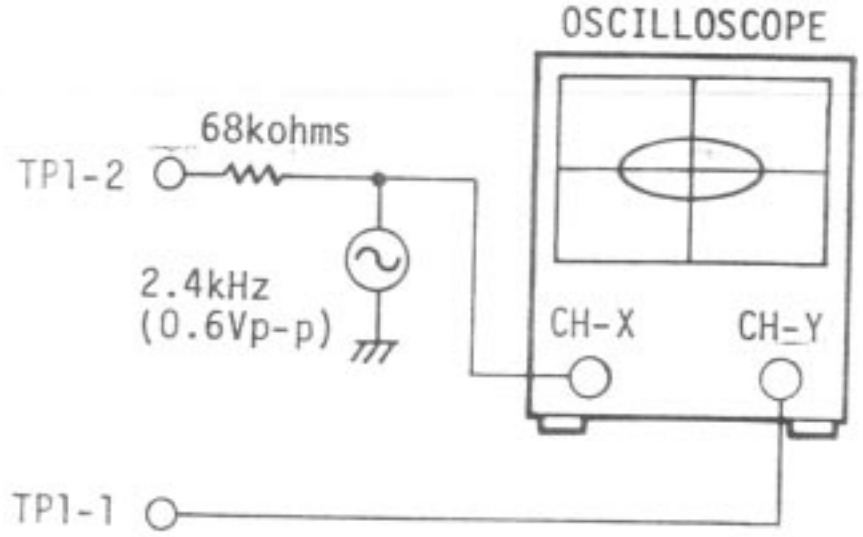


STEP NO.	MODE	SERVO LOOP	CHECK POINT	ADJUST. POINT	DETAIL
11	Play	TRKG: O/L TANG: O/L	pin 5 of Z504	VR504	**LOOP CLOSE TIMING IN SEARCH MODE/JCAB** Remove the N37 connector housing from the pin-post, and connect N37-7 (SCAN MODE) to GND. While observing the waveform at pin 5 of Z504 and the video signal at Video out terminal, adjust VR504 so that the center of DATA read-out duration is aligned with suppressed MCA code in the video signal. Disconnect N37-7 from GND, and connect the N37 connector housing to the pin-post again.

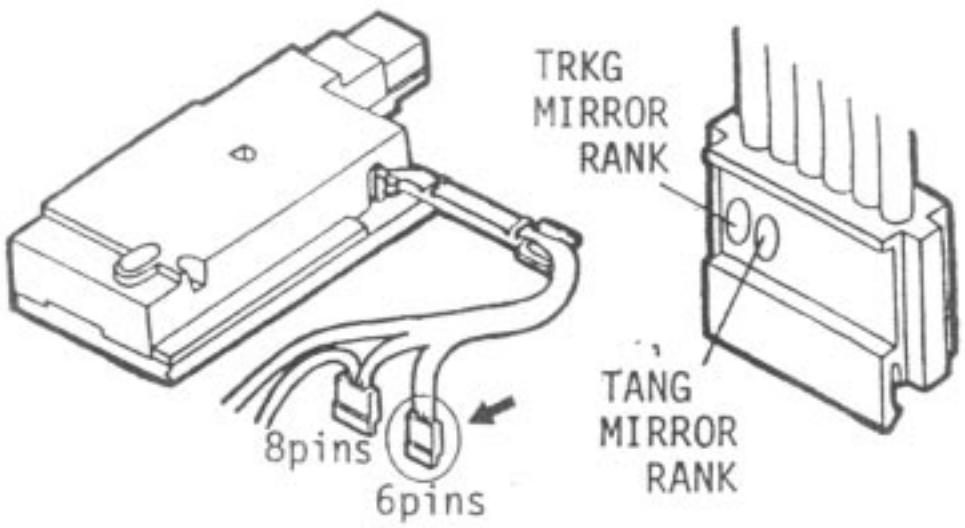


12	Scan rev.	TRKG: O/L TANG: O/L	—	VR3	**INSIDE LIMIT/JCAB** Connect a 220Ω resistor between pin 13 and pin 15 of Z202 on VSOP. While pressing SCAN REV key and observing the TV screen, adjust VR3 so that scan action ends in LEAD-IN no. 9—no. 11.
13	Scan rev.	TRKG: O/L TANG: O/L	—	VR4	**12/IN. DISC OUTSIDE LIMIT/JCAB** Connect a 220Ω resistor to the same position as step 12. While pressing SCAN FWD key and observing the TV screen, adjust VR4 so that scan action ends in LEAD-OUT no. 14—no. 16. Disconnect a resistor.

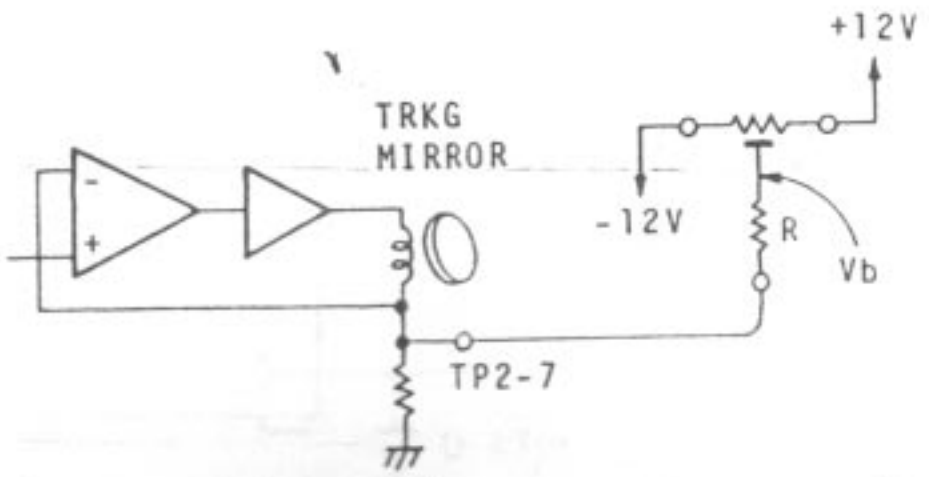
STEP NO.	MODE	SERVO LOOP	CHECK POINT	ADJUST. POINT	DETAIL
14	Still	TRKG: C/L TANG: O/L	pin 14 of Z6	VR5	**8/IN. DISC OUTSIDE LIMIT/JCAB** Scan fwd to the point where displayed Frame no. comes 24,000, and press STOP key. Adjust VR5 so that a voltage at pin 14 of Z6 on JCAB turns H to L. While playing in the vicinity of Frame no. 24,000, make sure that the voltage turns H to L in Frame no. 24,000—no. 24,300. Repeat this in several times.
15 STP 5	Play	TRKG: C/L TANG: O/L	TP1-1, TP1-2	VR2	**FOCS LOOP GAIN/VSOP** Disconnect TP2-8 from GND. Set the scope into X-Y mode and an oscillator output to 2.4 kHz (0.6 Vp-p). Connect the oscillator output to CH-X input and also to TP1-2 through a 68 kΩ, and connect CH-Y input to TP1-1. Adjust VR2 to make Lissajous figure into a holizontal ellipse.
16	Play	TRKG: C/L TANG: O/L	TP2-5 (VSOP), TP501-3	VR503	**TRKG LOOP GAIN/JCAB** Set the oscillator output to 4.8 kHz (10 Vp-p). Connect the output to CH-X input and also to TP501-3 through a 68 kΩ, and connect CH-Y input to TP2-5 (VSOP). Adjust VR503 to make lissajous figure into a holizontal ellipse.
17	Play	TRKG: C/L TANG: O/L	TP1-1	VR1	**FOCS LOOP OFFSET/VSOP** Play in the vicinity of Frame no. 100 nearby. While observing RF signal at TP2-11, adjust VR1 to obtain maximum RF signal. The measure an offset voltage of FOCS error at TP1-1 (DC voltage of the waveform center). Push REJECT key on the player, make sure that the voltage at TP1-1 is equal to that offset voltage. If not, adjust VR1.

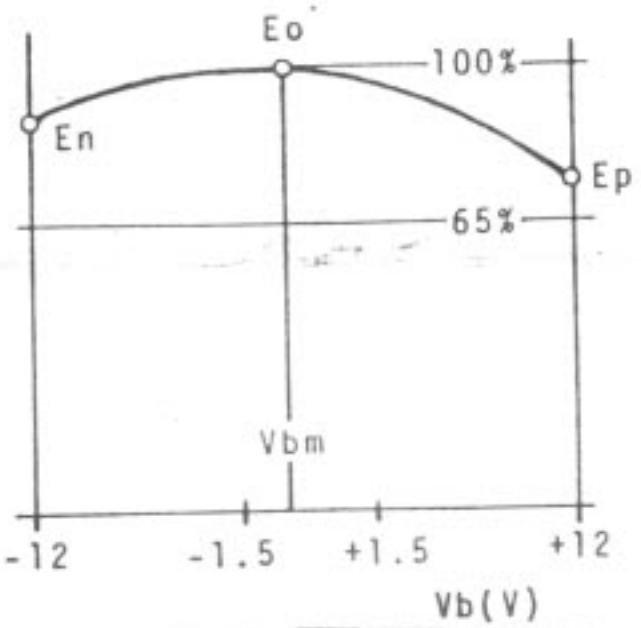


STEP NO.	MODE	SERVO LOOP	CHECK POINT	ADJUST. POINT	DETAIL
18	Play	TRKG: O/L TANG: O/L	–	–	**OPTICAL PATH CHECK/VSOP** This step has to be performed when the slider is replaced or the problem seems to relate with the optical path. Connect TP2-8 and TP3-1 to GND. TRKG and TANG mirrors are classified into five ranks by their sensitivities as shown below and their ranks are designated on the connector housing. Connect each end of jig VR to +12V and –12V line on VSOP, and also the center tap to TP2-7 through the resistor corresponding to the mirror rank. Adjust the jig VR to obtain maximum TRKG error at TP2-5, and read the peak-to-peak amplitude; Eo. Rotate the jig VR so that maximum positive bias is put to the mirror, and read the peak-to-peak amplitude; Ep. Rotate the jig VR so that maximum negative bias is put to the mirror, and read En. Make sure the followings. $Ep > 0.65 \times Eo$, $En > 0.65 \times Eo$ and $-1.5V < Vbm < +1.5V$ If $Ep > 0.80 \times Eo$ and $En > 0.80 \times Eo$, the Vbm is not confined to the above. Likewise, put bias to TANG mirror at TP2-12, and measure TRKG error peak-to-peak amplitudes Eo, Ep and En at TP2-5. Make sure that the before-mentioned standards are satisfied.

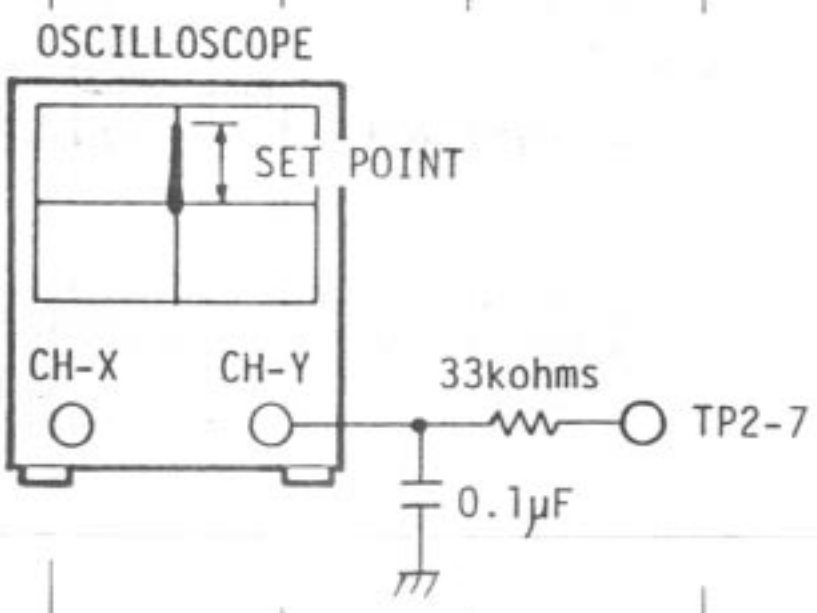


Mirror Rank			
Code	Color	No	R(Ohm)
C1	Black	1	316
C2	Red	2	300
C3	Yellow	3	273
D	Blue	4	240
E	Green	5	218



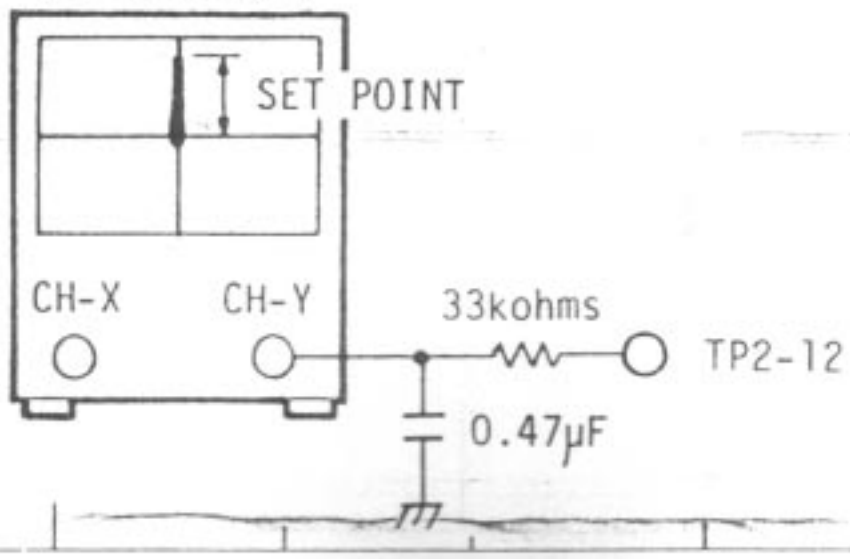


STEP NO.	MODE	SERVO LOOP	CHECK POINT	ADJUST. POINT	DETAIL
19	Scan fwd.	TRKG: C/L TANG: O/L	TP2-7	VR7	**TRKG MIRROR STOPPER/VSOP** Disconnect TP2-8 from GND. Set the scope into X-Y mode, and insert a low pass filter (33 kΩ/0.1 μF) between the probe and the scope input (CH-Y). While pressing SCAN FWD key, observe TP2-7 and adjust VR7 to obtain a positive voltage depending on the mirror rank. Mirror ranks and set points are shown below.
STP 0	ch 2				



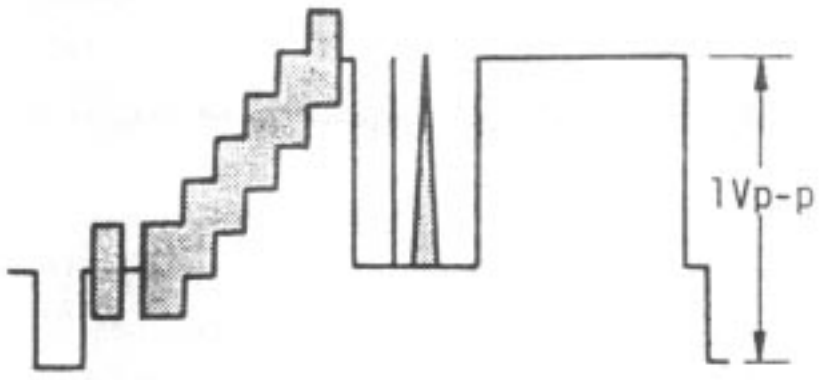
Mirror Rank			Set point (mV)
Code	Color	No	
C1	Black	1	200 ± 20
C2	Red	2	210 ± 20
C3	Yellow	3	230 ± 20
D	Blue	4	250 ± 20

20	Play	TRKG: C/L TANG: C/L	TP3-4	VR401	**TANG COMPENSATION IN V-BLANKING INTERVAL/VSOP** Disconnect TP2-8 and TP3-1 from GND. While observing TANG error at TP3-4 and the video signal, adjust VR401 to minimize the TANG error waveform in the vertical blanking interval of the video signal.
STP 9	ch 2				
21	Play	TRKG: C/L TANG: C/L, O/L	TP2-12	VR405	**TANG MIRROR STOPPER/VSOP** Insert a low pass filter (33 kΩ/0.47 μF) between the probe and the scope input. Rotate VR405 fully CW direction, and adjust VR404 so that a voltage at TP2-12 comes the set point X. (shown below) Rotate VR405 slowly to CCW direction and adjust to the set point Y. . Connect TP3-1 to GND, and adjust so that a voltage at TP2-12 comes 0±20 mV.
STP 0	ch 1				

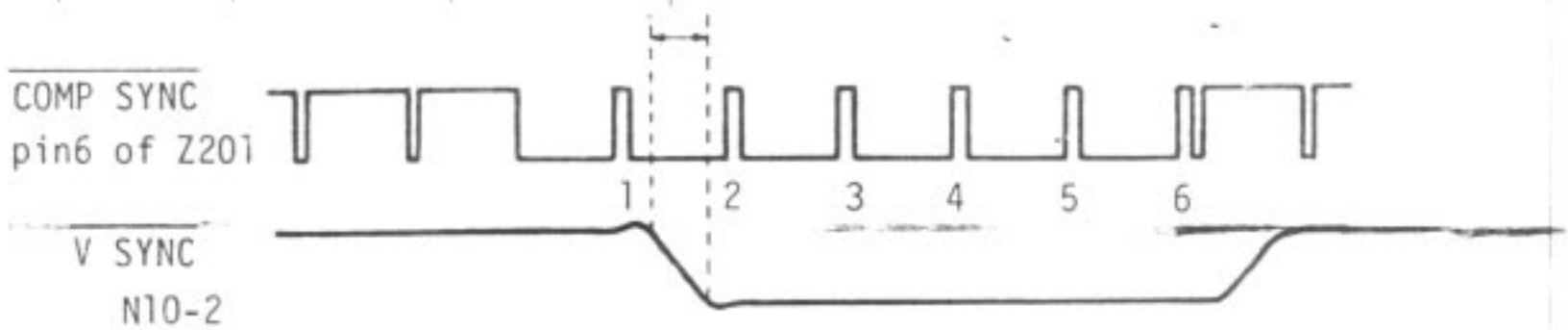


Mirror Rank			Set point	
Code	Color	No	X(V)	Y(V)
C1	Black	1	-0.55	-0.40
C2	Red	2	-0.60	-0.45
C3	Yellow	3	-0.65	-0.50
D	Blue	4	-0.70	-0.55
E	Green	5	-0.80	-0.65

STEP NO.	MODE	SERVO LOOP	CHECK POINT	ADJUST. POINT	DETAIL
22	Still	TRKG: C/L TANG: C/L	Video out	VR201	**VIDEO OUTPUT LEVEL/VSOP** Disconnect TP2-9 and TP3-1 from GND. Play in the vicinity of Frame no. 1,000 nearby, and push STOP key where the composite test signal is reproduced. With Video output terminated into 75Ω, make sure that the video level is 1±0.1V from the sync tip to the white peak. If not, adjust VR201 to satisfy the above.
23	Still	TRKG: C/L TANG: C/L	pin 16, 18 of Z201	VR202	**1H DELAYED VIDEO LEVEL/VSOP** Make sure that the video level at pin 16 of Z201 is equal to the level at pin 18. If not, adjust VR202.
24	Play	TRKG: C/L TANG: C/L	pin 6 of Z201, N10-2	VR203	**V SYNC TRAILING EDGE TIMING/VSOP** Make sure that V SYNC trialing edge is aligned with the position between the first and second equalizing pulses in COMP SYNC (pin 6 of Z201) after that trailing edge. If not, adjust VR203.

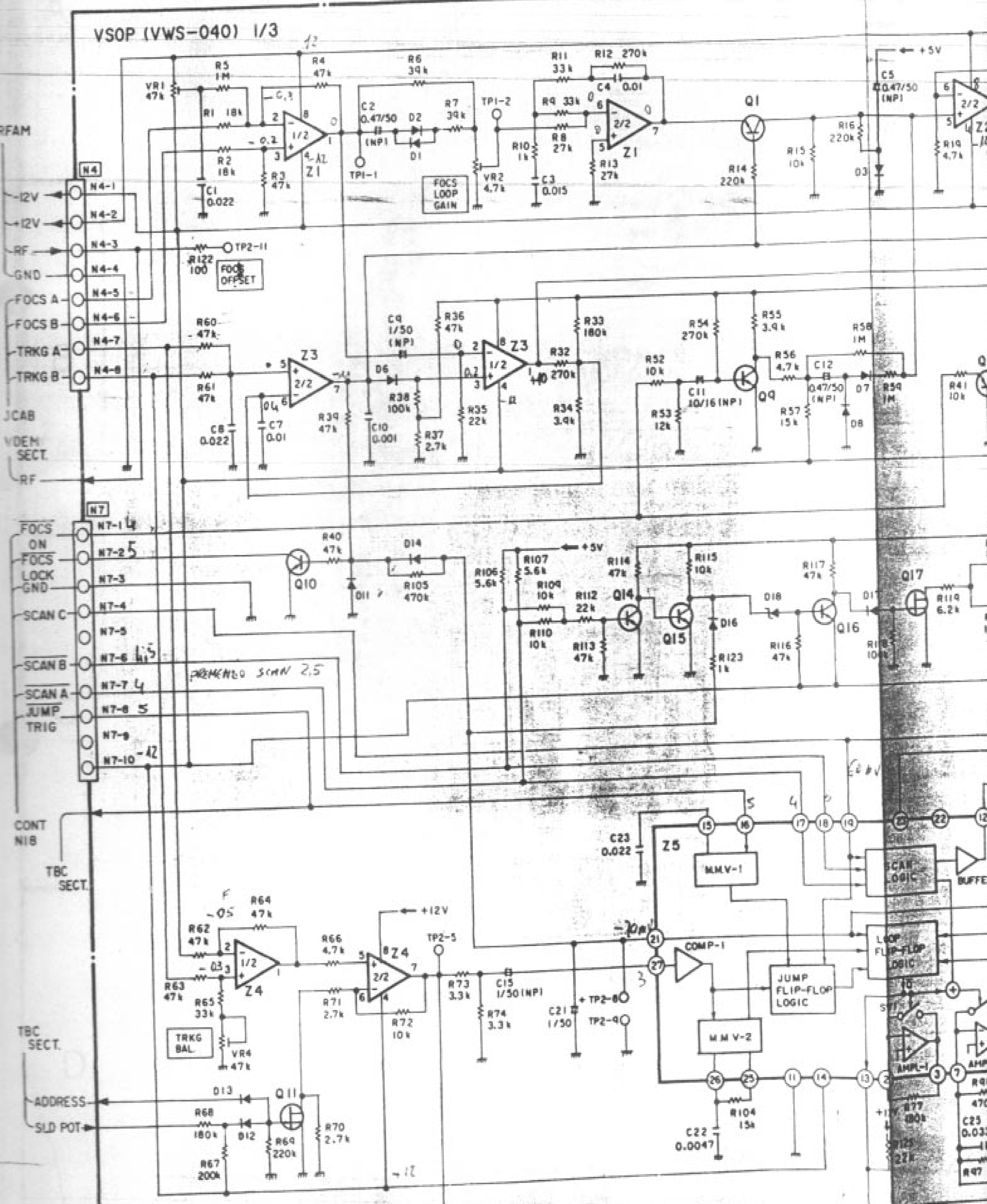


COMPOSITE TEST SIGNAL



STEP NO.	MODE	SERVO LOOP	CHECK POINT	ADJUST. POINT	DETAIL
25	Play	TRKG: C/L TANG: O/L	TP3-2, TP3-3	VR406	**SPDL LOOP OFFSET/VSOP** Connect TP3-1 to GND. Adjust VR406 so that the center of the leading edge of PB H including jitter (at TP3-2) is aligned with the leading edge of REF H (at TP3-3). After about 30 seconds, make sure that a phase difference between PB H and REF H is less than ±2μseconds. If it is greater, then adjust VR406 again. Disconnect TP3-1 from GND, and make sure that there is no red streak or other color distortion in the picture.
26	Play	TRKG: C/L TANG: C/L	Audio out	VR1, VR2	**AUDIO OUTPUT LEVEL/JCAB** While playing from Frame no. 25,201 to no. 26,100, adjust VR1 so that the CH1/L audio signal level at Audio out put terminal with terminated into 51 kΩ comes 490±60 Vrms. While playing from Frame no. 26,101 to no. 27,000, adjust VR2 so that the CH2/R level comes 490±60 Vrms.

6. VSOP AND CPCB



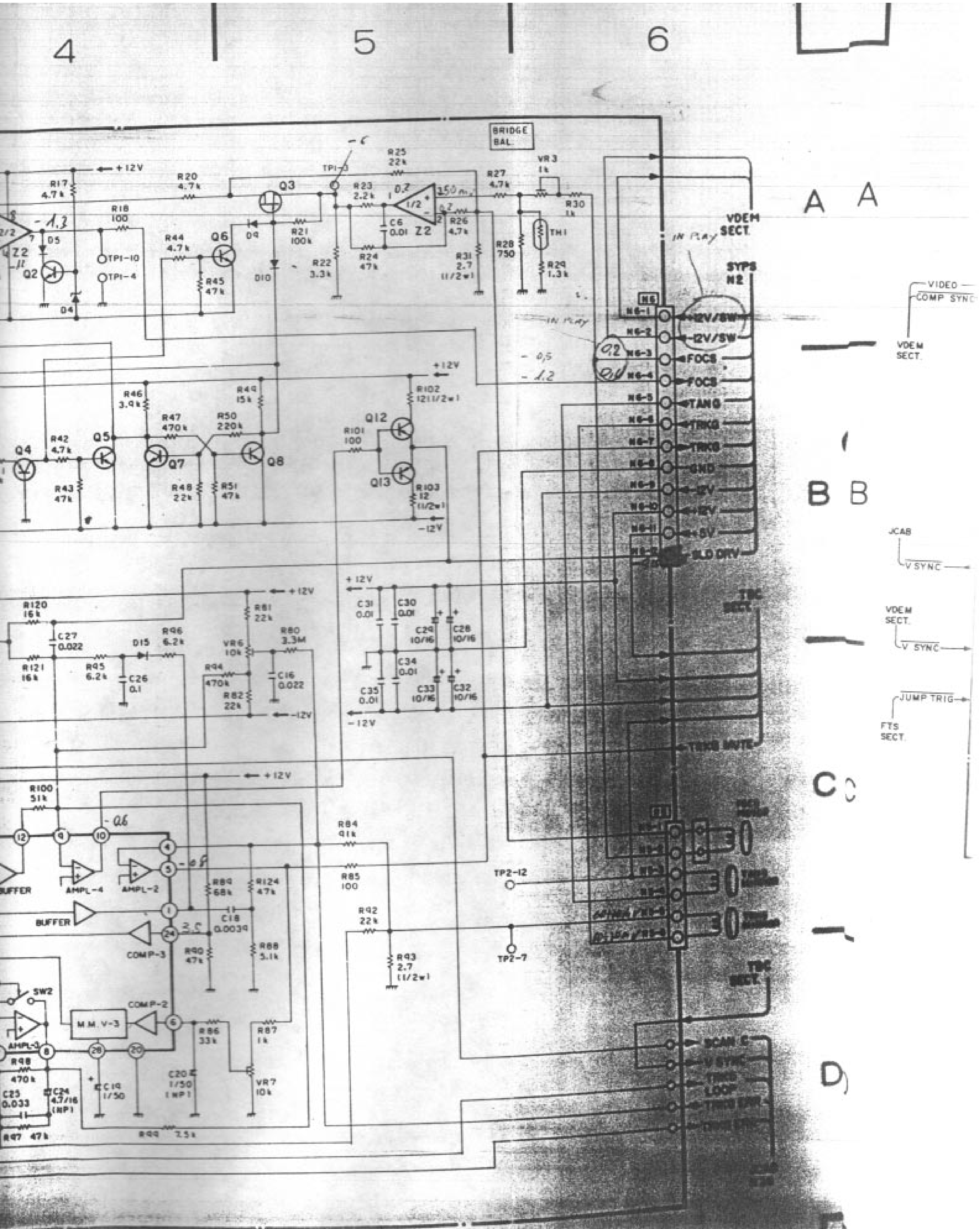
Z1,4 : μPC4558C
Z2 : μPC4559C
Z3 : μPC393C
Z5 : UM004

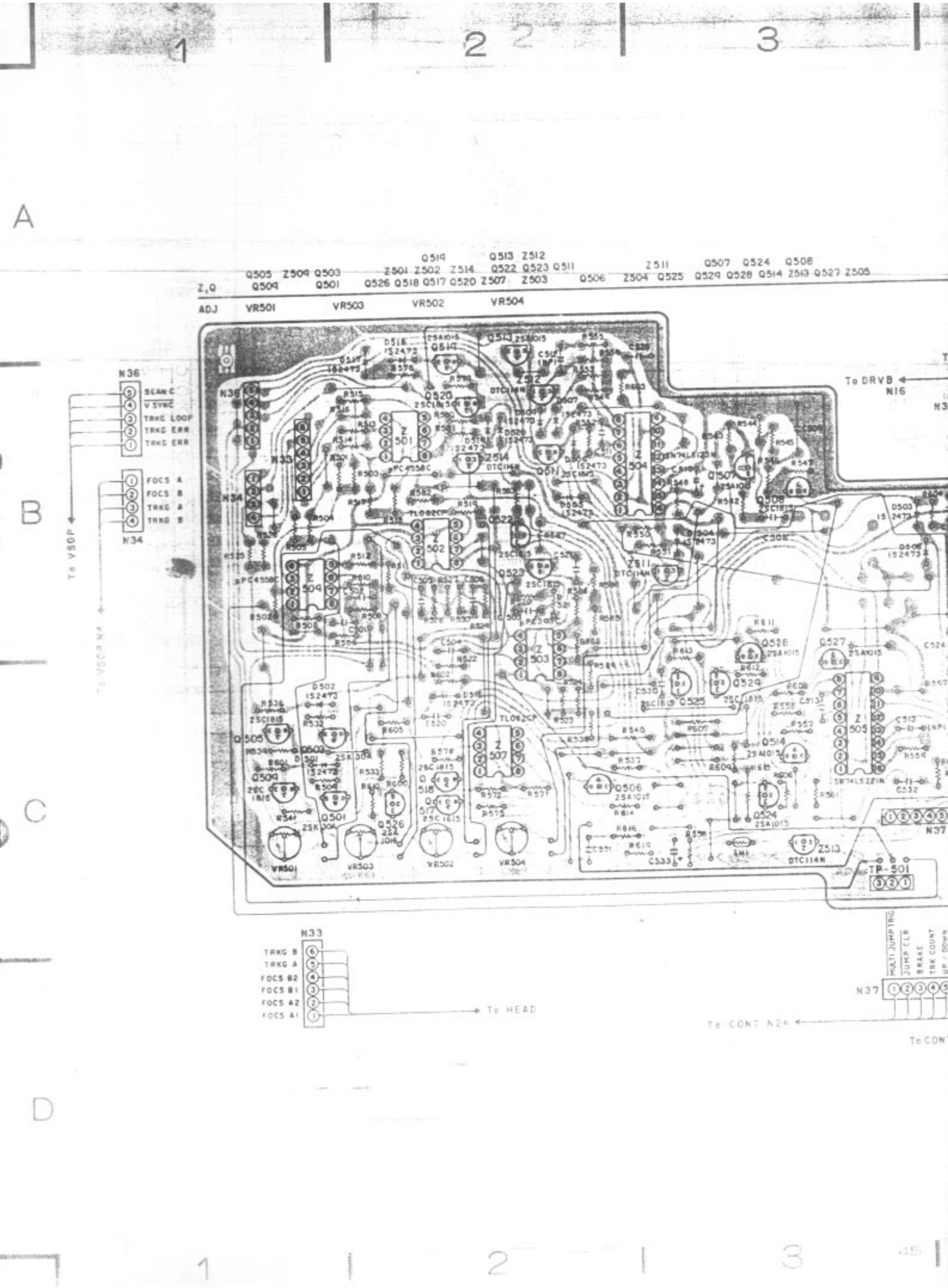
D1,2 : 1K60
D4 : WZ-090
D18 : WZ-150
OTHERS : 1S2473

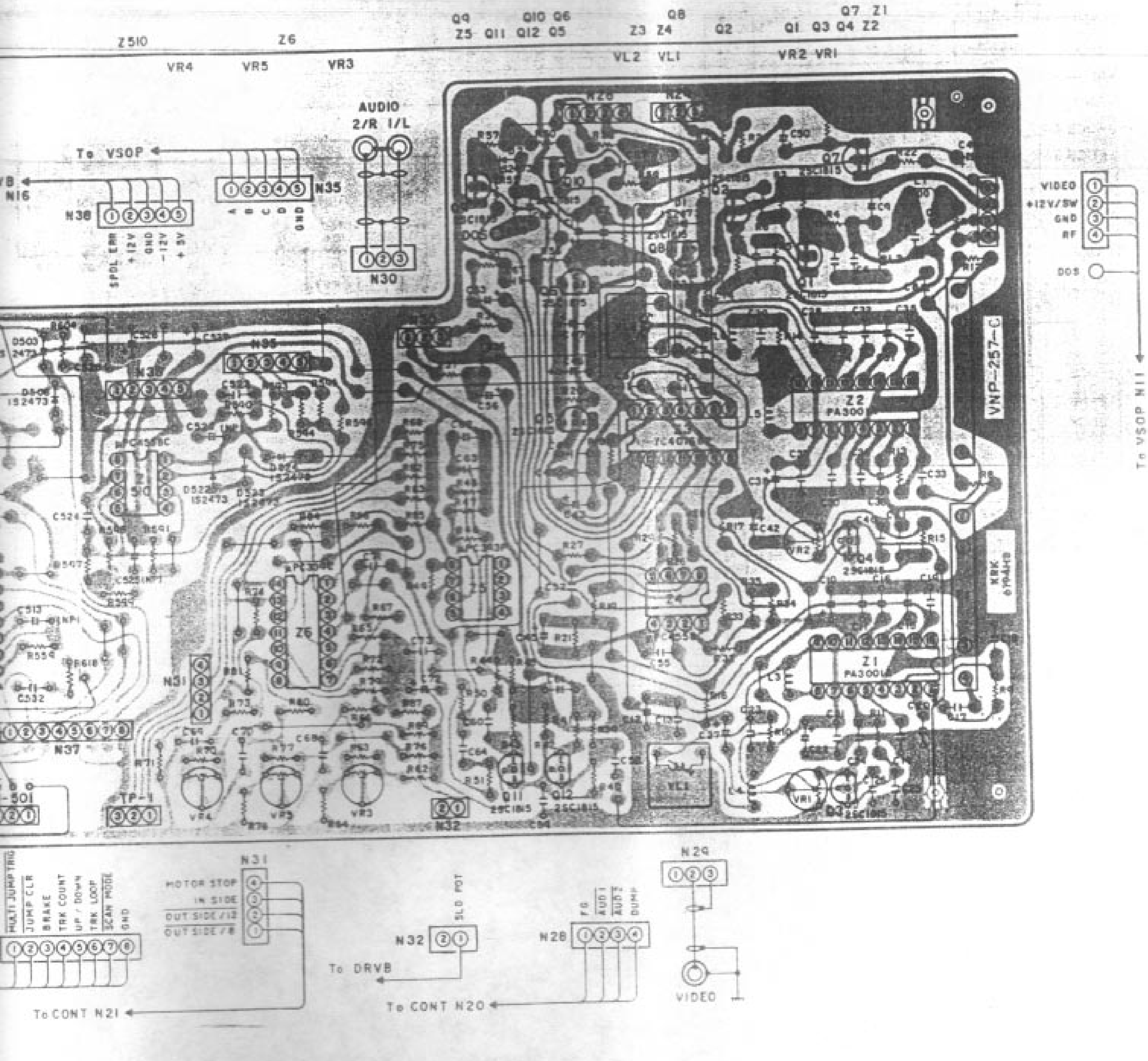
Q12 : 2SC495
Q13 : 2SA505

OTHERS NPN : 2SC1815

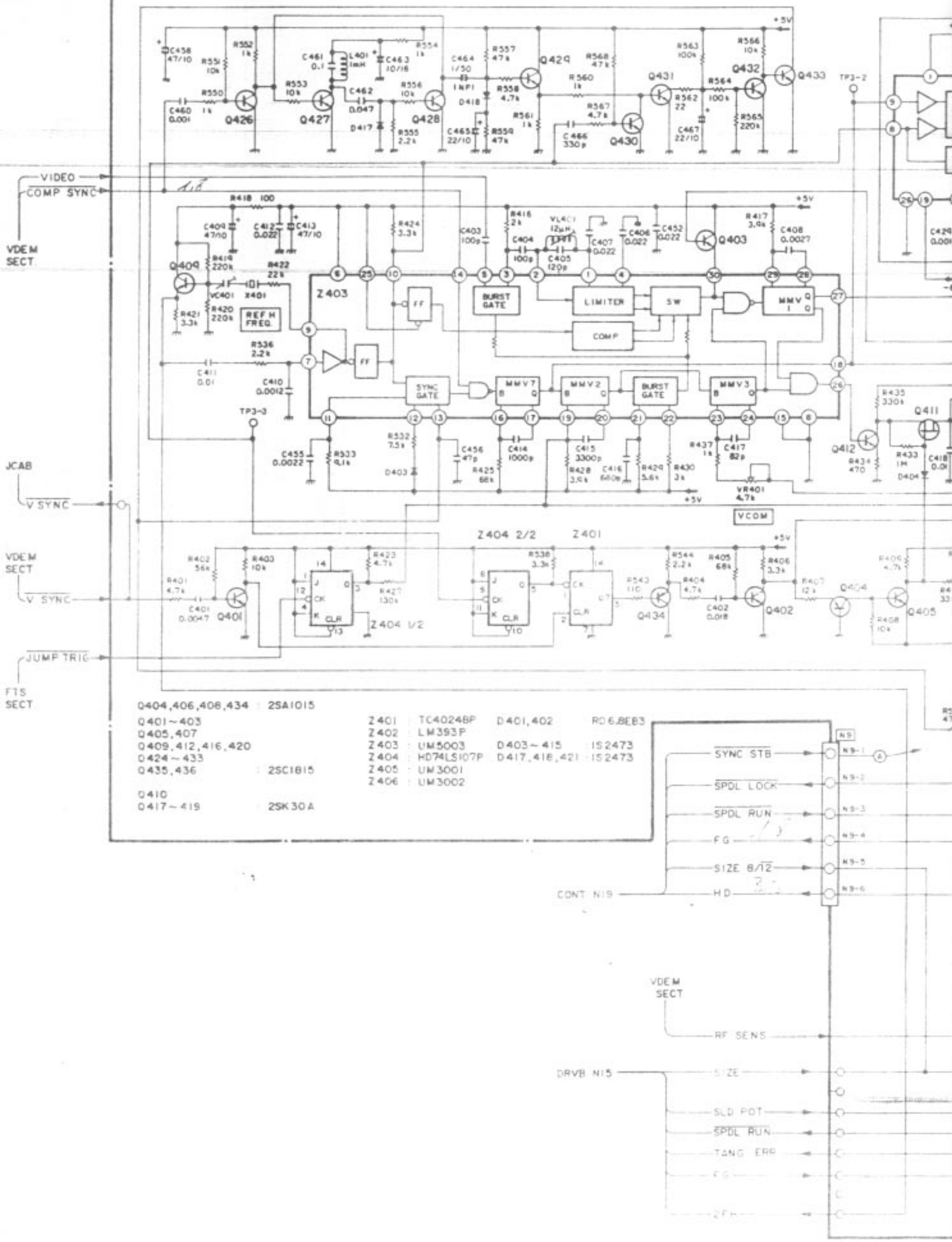
PNP : 2SA1015
FET : 2SK30


4
5
6
A
B
C
D
BRIDGE BAL.
VDEM SECT.
SYPS N2
TBC SECT.
TRKG MUTE
VIDEO
COMP SYNC
VDEM SECT.
JCAB
V SYNC
V SYNC
JUMP TRIG
FTS SECT.
+12V
-12V
Q3
Q4
Q5
Q6
Q7
Q8
Q12
Q13
Z2
BUFFER
AMPL-4
AMPL-2
AMPL-3
COMP-3
COMP-2
M.M. V-3
SW2
TP2-12
TP2-7
12V/SW
FOCS
TANG
TRKG
GND
-12V
+12V
+5V
SLD DRV
SCAN C
V SYNC
TRKG LOOP
IN PLAY


Z,Q
ADJ
VR501
VR503
VR502
VR504
N36
SCAN C
V SYNC
TRKG LOOP
TRKG ERR
TRKG ERR
N34
FOCS A
FOCS B
TRKG A
TRKG B
To VSOP
To DRVB
N16
N33
TRKG B
TRKG A
FOCS B2
FOCS B1
FOCS A2
FOCS A1
To HEAD
N37
MULTI JUMP TRG
JUMP CLR
BRAKE
TRK COUNT
UP / DOWN
To CONT N24
TP-501


4
5
A
B
C
D
Q9
Z5 Q11
Q10 Q6
Q12 Q5
Z3 Z4
Q8
Q2
Q7 Z1
Q1 Q3 Q4 Z2
Z510
Z6
VR4
VR5
VR3
VL2 VL1
VR2 VR1
AUDIO
2/R 1/L
To VSOP
N35
N36
N30
N16
VIDEO
+12V/SW
GND
RF
DOS
To VSOP N11
VNP-257-C
PA3001
N37
N31
N32
TP-1
MULTI JUMP TRIG
JUMP CLR
BRAKE
TRK COUNT
UP / DOWN
TRK LOOP
SCAN MODE
GND
To CONT N21
MOTOR STOP
IN SIDE
OUT SIDE/12
OUT SIDE/8
SLD POT
To DRVB
N28
To CONT N20
N29
VIDEO

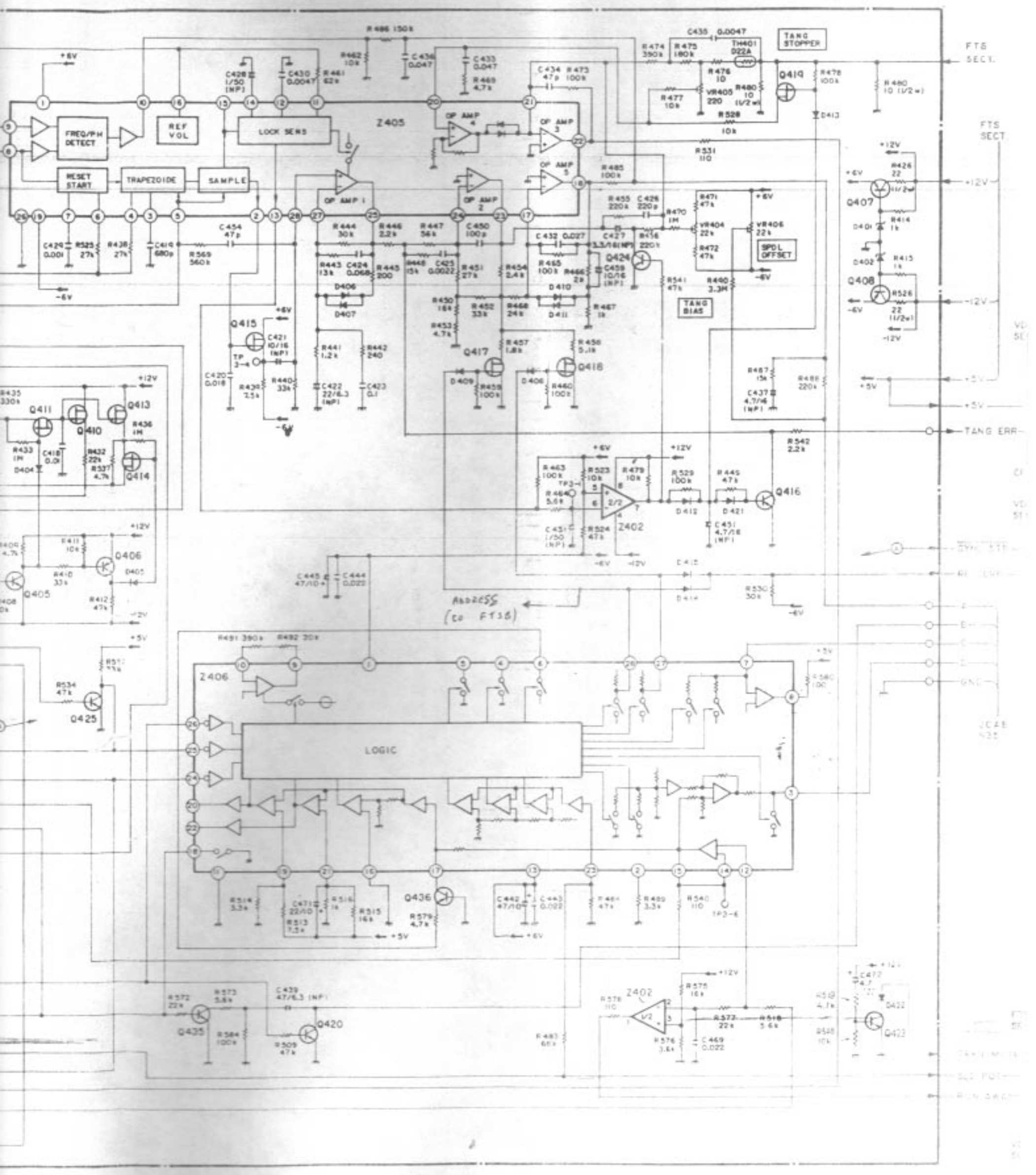
VSOP (VWS-040) 2/3



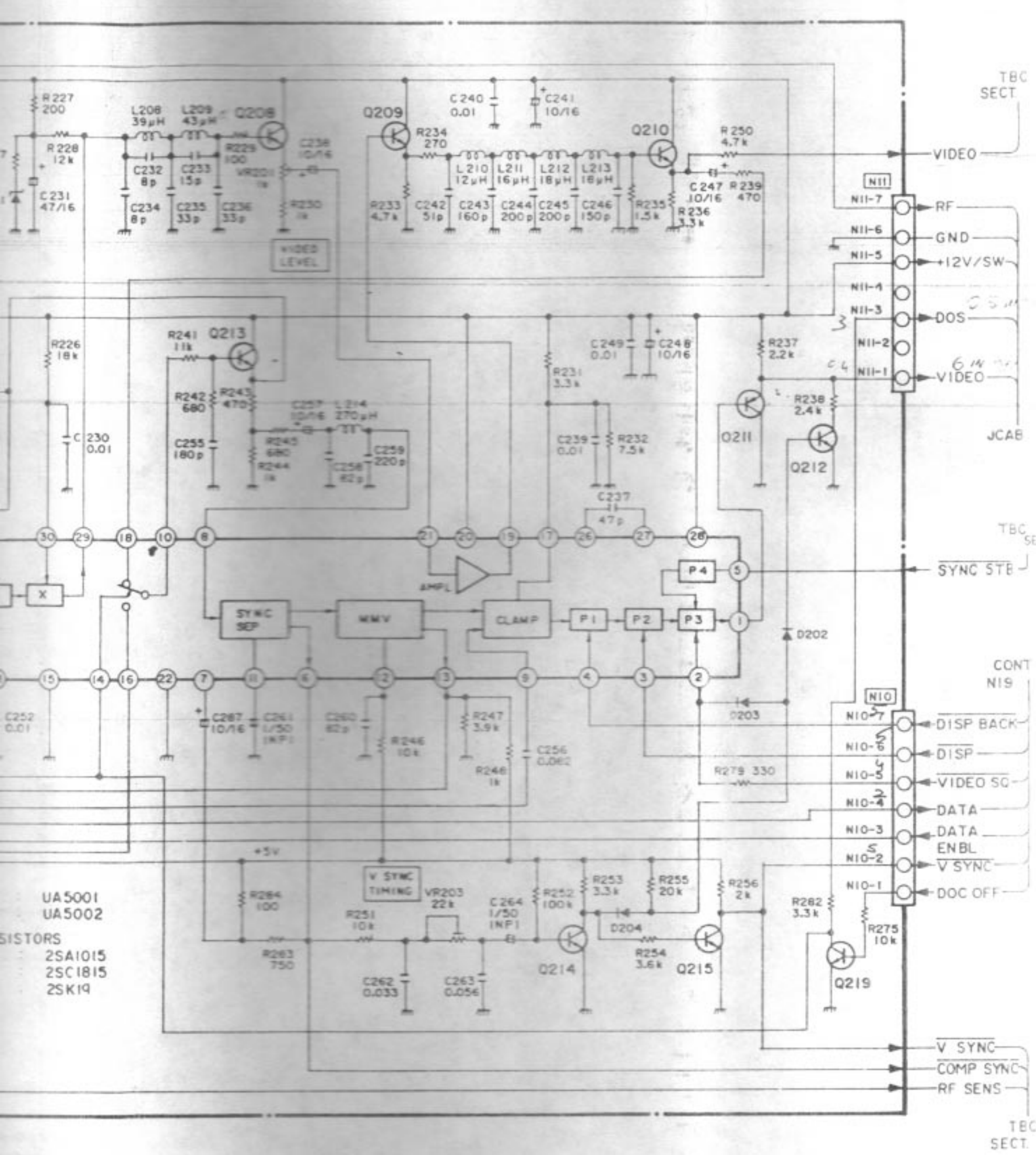
Q404,406,408,434 : 2SA1015
Q401~403
Q405,407
Q409,412,416,420
Q424~433
Q435,436 : 2SC1815
Q410
Q417~419 : 2SK30A

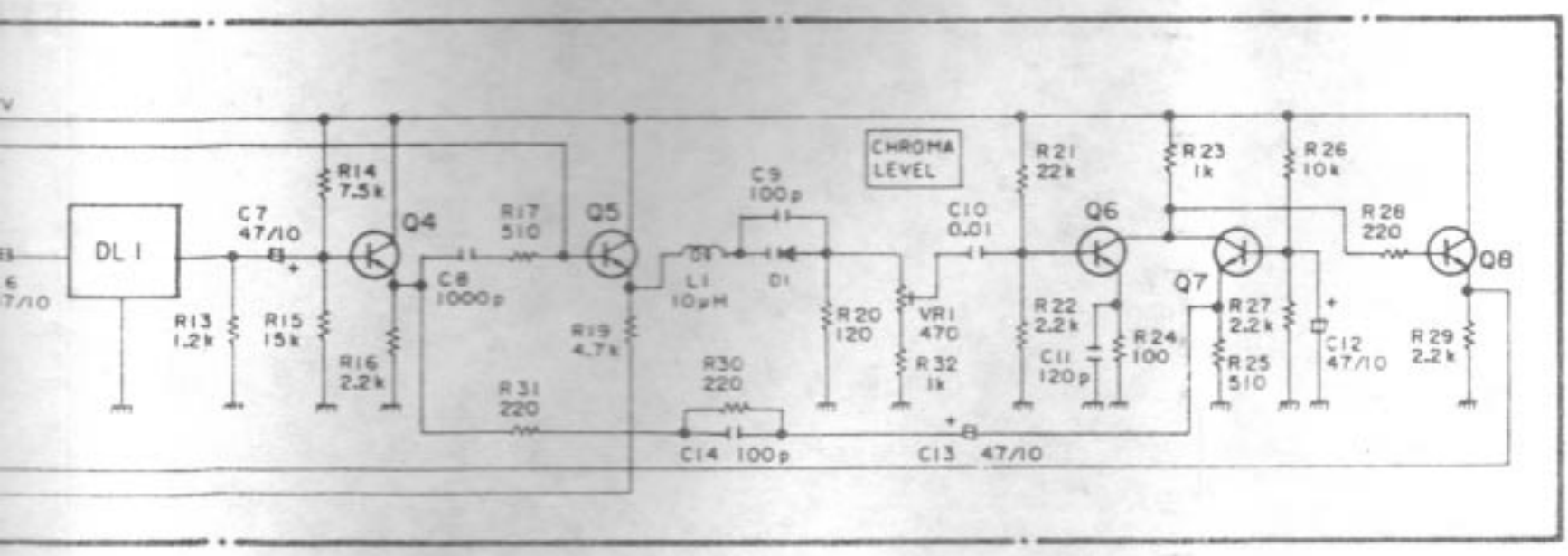
Z401	TC40248P	D401,402	RD6.8EB3
Z402	LM393P		
Z403	UM5003	D403~415	IS2473
Z404	HD74LS107P	D417,418,421	IS2473
Z405	UM3001		
Z406	UM3002		

A
B
C
D
1
2
3


FREQ/PH DETECT
REF VOL
LOCK SENS
RESET START
TRAPEZOIDE
SAMPLE
Z405
OP AMP 1
OP AMP 2
OP AMP 3
OP AMP 4
OP AMP 5
TANG STOPPER
SPDL OFFSET
TANG BIAS
Q407
Q408
Q410
Q411
Q413
Q414
Q415
Q416
Q417
Q418
Q424
Q425
Q436
Q439
Q420
Z402
Z406
LOGIC
FTS SECT.
TANG ERR
Address (to FTS6)

VSOP (VWS-040) 3/3
+12V/SW
RF
FTS SECT.
Q201
Q202
Q204
Q205
Q206
DL-201 1H DELAY
Q203
Q216
Q207
Q217
Q218
IRF CORR
RUN AWAY
+5V
TBC SECT.
VR204
VR202
D205
D206
D207
D208
DOS TIMING
Z202
MMV-1
MMV-2
LIM
DSCRM
AMPL
CLAMP & SLICE
Z201
L1M
X
TANG ERR
+12V
-12V
FTS SECT.
CPCB (VWV-028)
N26
Q1,2, 4~8 : 2SC1815
Q3 : 2SA1015
D1 : SVC321SP
Z201 UA5
Z202 UA5
TRANSISTORS
PNP 2SA
NPN 2SC
FET 2SK


R227 200
L208 39µH
L209 43µH
Q208
R228 12k
C231 47/16
C232 8p
C233 15p
R229 100
VR201 1k
C234 8p
C235 33p
C236 33p
C238 10/16
R230 1k
VIDEO LEVEL
Q209
R234 270
C240 0.01
C241 10/16
Q210
R250 4.7k
L210 12µH
L211 16µH
L212 18µH
L213 18µH
R233 4.7k
C242 51p
C243 160p
C244 200p
C245 200p
C246 150p
R235 1.5k
C247 10/16
R239 470
R236 3.3k
TBC SECT
VIDEO
N11
N11-7
RF
N11-6
GND
N11-5
+12V/SW
N11-4
N11-3
DOS
N11-2
N11-1
VIDEO
JCAB
R226 18k
R241 11k
Q213
R242 680
R243 470
C257 10/16
L214 270µH
C255 180p
R245 680
R244 1k
C258 82p
C259 220p
C230 0.01
R231 3.3k
C249 0.01
C248 10/16
R237 2.2k
R238 2.4k
Q211
Q212
C239 0.01
R232 7.5k
C237 47p
30
29
18
10
8
21
20
19
17
26
27
28
X
AMPL
P4
5
TBC SECT
SYNC STB
SYNC SEP
MMV
CLAMP
P1
P2
P3
1
D202
15
14
16
22
7
11
6
2
3
9
4
3
2
C252 0.01
C267 10/16
C261 1/50 (NP1)
C260 82p
R246 10k
R247 3.9k
C256 0.082
R248 1k
D203
CONT NI9
N10
N10-7
DISP BACK
N10-6
DISP
R279 330
N10-5
VIDEO SQ
N10-4
DATA
N10-3
DATA ENBL
N10-2
V SYNC
N10-1
DOC OFF
+5V
R264 100
V SYNC TIMING
VR203 22k
R251 10k
R263 750
C262 0.033
C263 0.056
C264 1/50 (NP1)
R252 100k
R253 3.3k
R255 20k
R256 2k
D204
R254 3.6k
Q214
Q215
R282 3.3k
R275 10k
Q219
V SYNC
COMP SYNC
RF SENS
TBC SECT
UA5001
UA5002
SISTORS
2SA1015
2SC1815
2SK19


R14 7.5k
C7 47/10
Q4
R17 510
Q5
C9 100p
CHROMA LEVEL
C10 0.01
R21 22k
R23 1k
R26 10k
Q6
R28 220
Q8
DL 1
C8 1000p
L1 10µH
D1
Q7
R13 1.2k
R15 15k
R16 2.2k
R19 4.7k
R20 120
VR1 470
R32 1k
R22 2.2k
C11 120p
R24 100
R27 2.2k
R25 510
C12 47/10
R29 2.2k
R30 220
R31 220
C14 100p
C13 47/10

4 5 6