

Regulator/Audio II PCB Schematic (035435-02 B)

The Regulator/Audio PCB has the dual functions of regulating the +5 VDC logic power to the game PCB and amplifying the audio from the game PCB.

Regulator Circuit

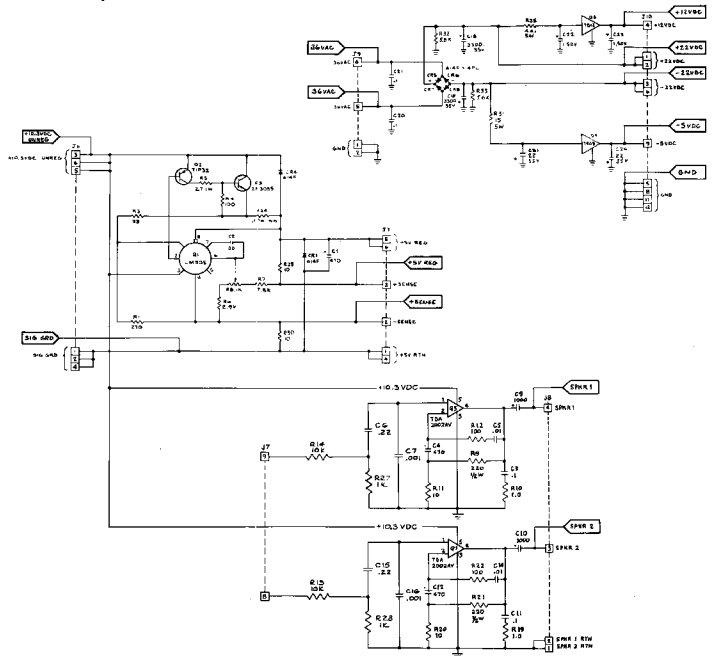
The regulator consists of voltage regulator Q1, current source power transistor Q3 and Q3's bias transistor Q2. The regulator accurately regulates the logic power input to the game PCB by monitoring the voltage through high impedance inputs +SENSE and -SENSE. The inputs are directly from the +5 VDC and ground inputs to the game PCB. Therefore, the regulator regulates the voltage on the game PCB. This eliminates a reduced voltage due to IR buildup on the wire harness between the regulator and the game PCB. Variable resistor R8 is adjusted for the +5 VDC on the game PCB. Once adjusted, the voltage at the input of the game PCB will remain constant at this voltage.

Regulator Adjustment

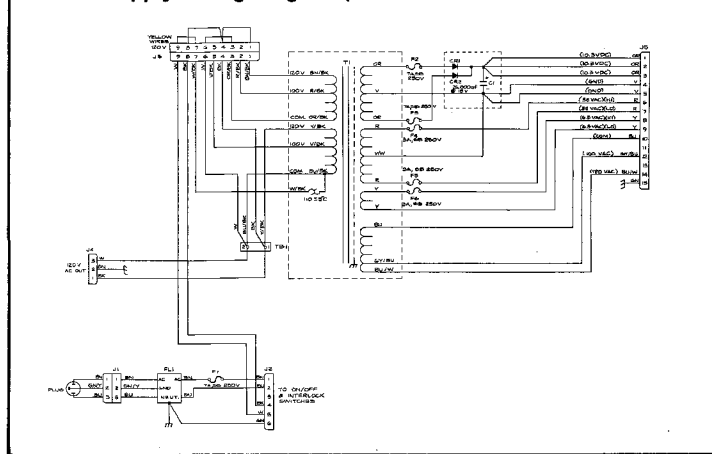
1. Connect a voltmeter between +5 V and GND test points of the game PCB.
2. Adjust variable resistor R8 on the Regulator/Audio PCB for +5 VDC reading on the voltmeter.
3. Connect a voltmeter between +5 V REG and GND on the Regulator/Audio PCB. Voltage reading shall not be greater than +5.5 VDC. If greater, try cleaning edge connectors on both the game PCB and the Regulator/Audio PCB.
4. If cleaning PCB edge connectors doesn't decrease voltage difference, connect minus lead of voltmeter to GND test point of Regulator/Audio PCB and plus lead to GND test point of game PCB. Note the voltage. Now connect minus lead of voltmeter to +5 REG test point on Regulator/Audio PCB and plus lead to +5 V test point on game PCB. From this you can see which harness circuit is dropping the voltage. Troubleshoot the appropriate harness wire or harness connector.

Audio Circuit

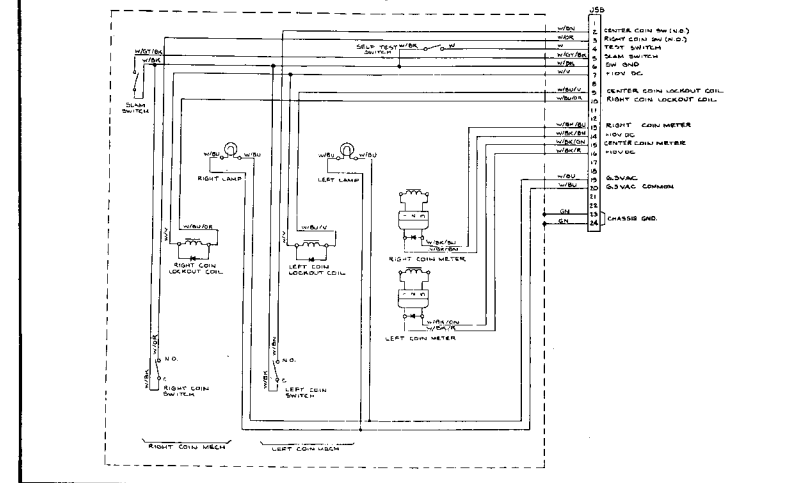
The audio circuit contains two independent audio amplifiers. Each consists of a TDA2002AV amplifier with a gain of ten.



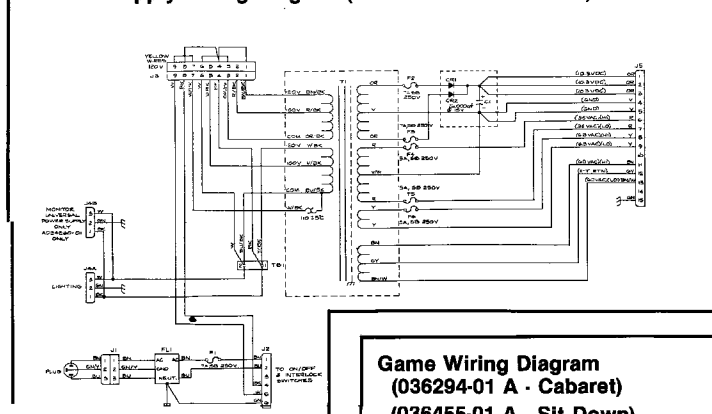
Power Supply Wiring Diagram (036097-01 B Cabaret)



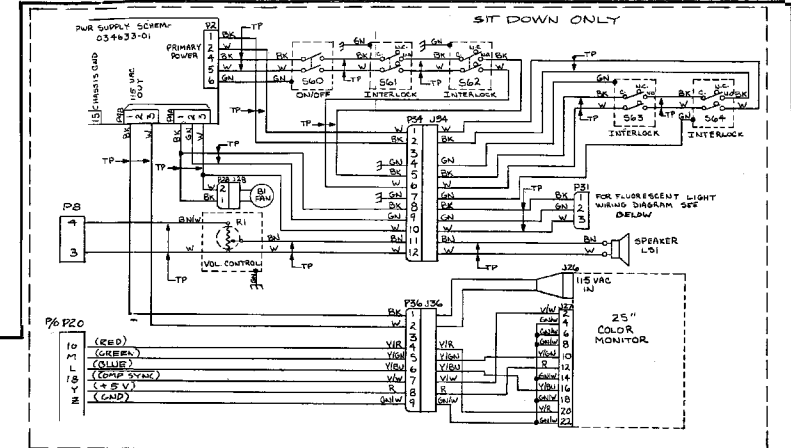
Coin Door Schematic (034988-01 A)



Power Supply Wiring Diagram (034633-01 B Sit Down)



Game Wiring Diagram (036294-01 A - Cabaret) (036455-01 A - Sit Down)



Drawing Package Supplement

to

MISSILE COMMAND™

Operation, Maintenance, and Service Manual

DIAGNOSTIC TESTS

Instruction	Use of Test
1. Set self-test switch to on position. Note: entering self-test will set the HIGH SCORE TODAY display to 7500.	
2. Press alpha base fire button and slam switch simultaneously. Release slam switch first.	A convergence pattern appears on the monitor screen. The background can be many possible colors. If you are going to converge the monitor, black is the color you want. To change background color, press either START button. Do not attempt any convergence adjustments unless you are a qualified color TV technician!
3. Press omega base fire button and slam switch simultaneously. Release slam switch first.	Vertical color bars appear on the screen, to permit color hue and brightness adjustments. Pressing either start button changes the color of the right and left vertical bars. Do not attempt any color hue or brightness adjustments unless you are a qualified color TV technician!
4. Press delta base fire button and slam switch simultaneously.	White screen appears, and tiny black dots trace all the raster lines from top to bottom (takes about 67 seconds). After this, a blue RAM OK message appears on the screen, and the + will reappear. If the message BAD RAM appears and some or all of the digits 1 thru 8, refer to the following to determine the failing RAM chips.
5. Set self-test switch to off position.	Check attract mode display and readjust brightness if necessary.

Test no. 4 display	Bad chip location
BAD RAM 8	R4
BAD RAM 7	N4
BAD RAM 6	M4
BAD RAM 5	L4
BAD RAM 4	K4
BAD RAM 3	J4
BAD RAM 2	H4
BAD RAM 1	F4

Contents of this Drawing Package

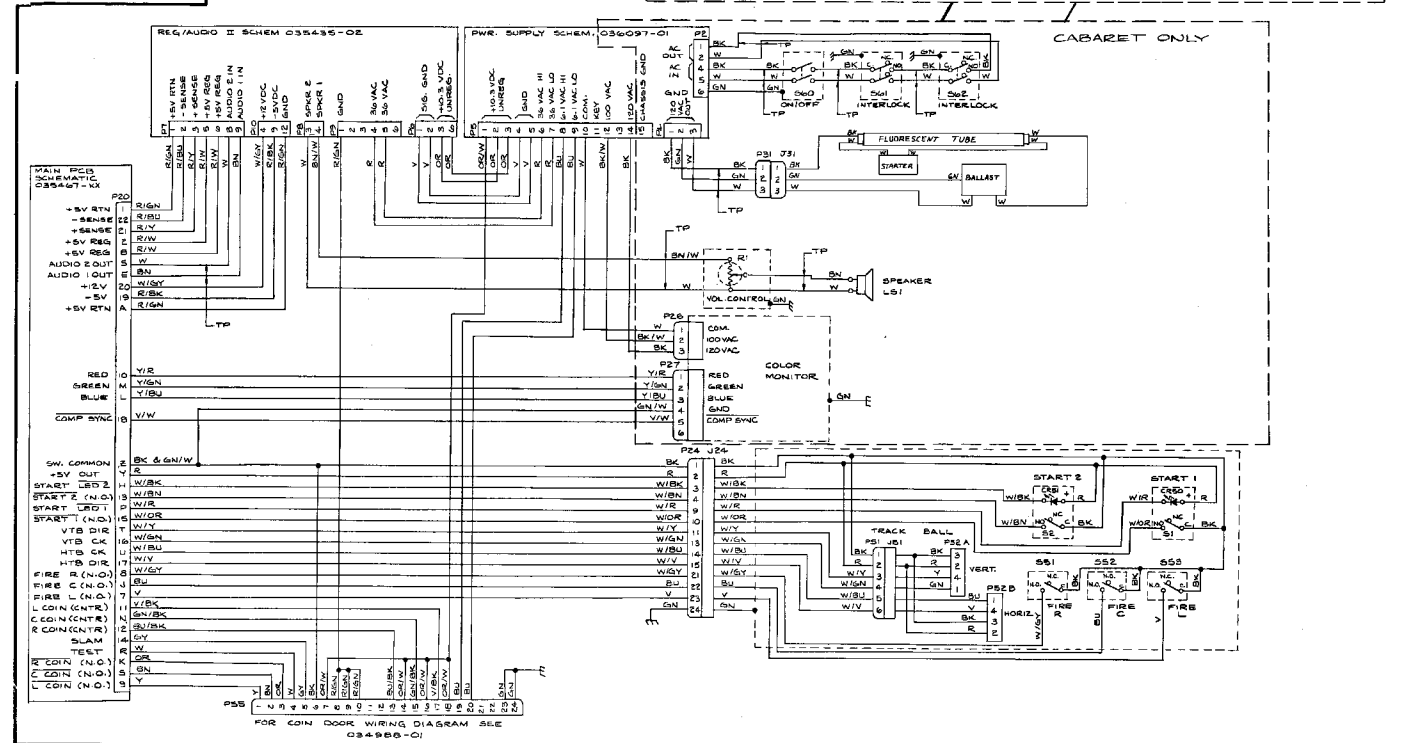
Game Wiring Diagram, Coin Door and Power Supply Microprocessor and Sync Video Generator Input and Output Circuitry

Sheet 1, Side A
Sheet 1, Side B
Sheet 2, Side A
Sheet 2, Side B



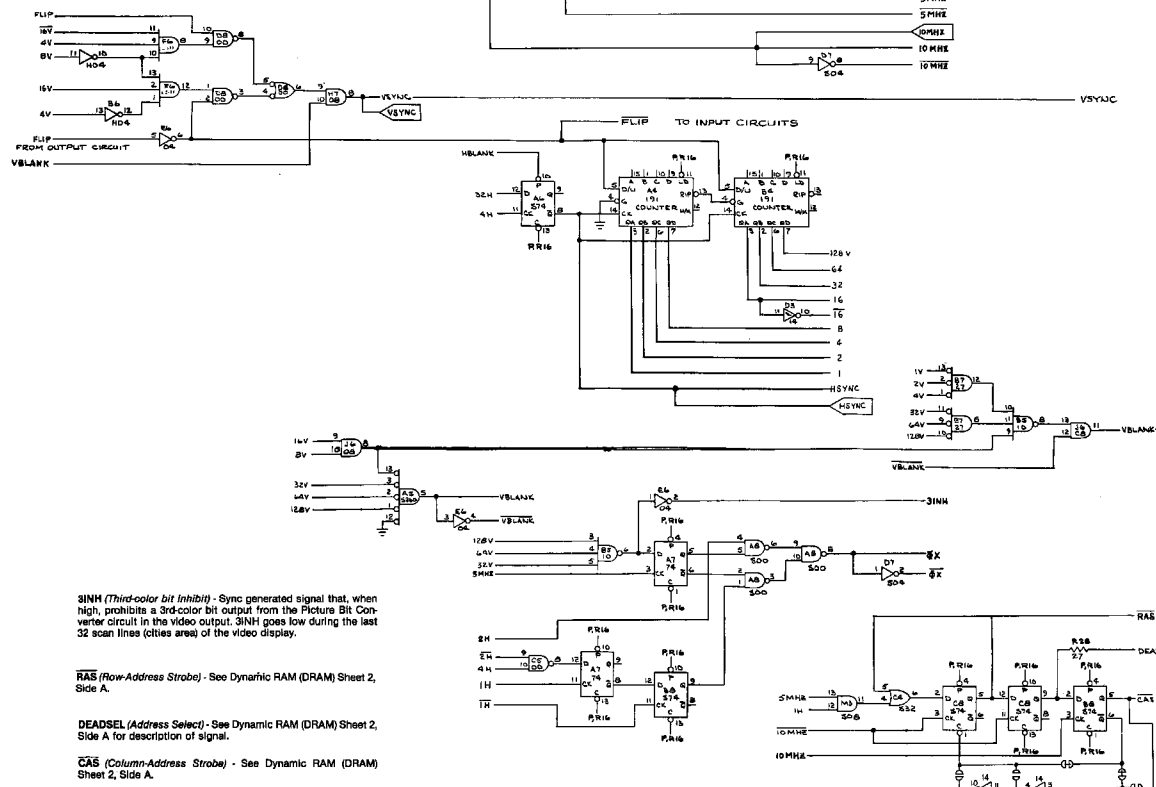
Atari Home Communications Company

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Sync

FLIP (Video Inverse Enable) - Microprocessor-generated signal clocked by Address Decode **OUT0**, used in Missile Command Cocktail game only. High FLIP reverses count output of vertical sync signal and relocates VSYNC signal, inverting Cocktail game video picture. Cocktail game must have 02 or later Program Memory installed.



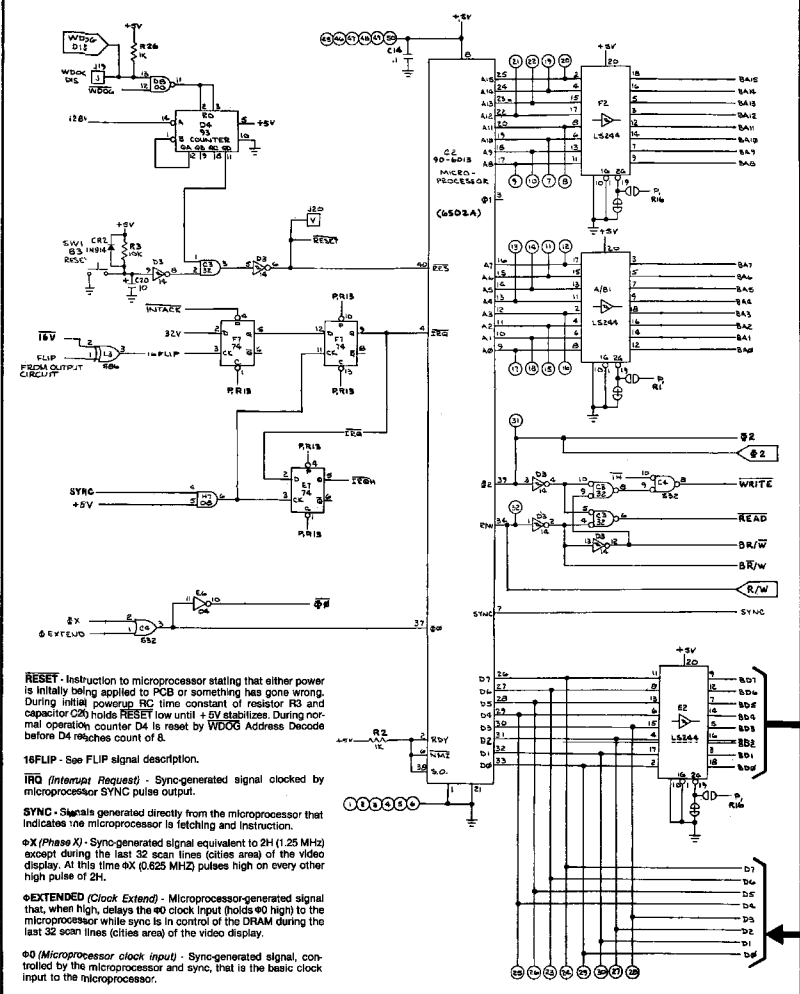
3INH (Third-color bit Inhibit) - Sync generated signal that, when high, prohibits a 3rd-color bit output from the Picture Bit Converter circuit in the video output. 3INH goes low during the last 32 scan lines (cites area) of the video display.

RAS (Row-Address Strobe) - See Dynamic RAM (DRAM) Sheet 2, Side A.

DEADSEL (Address Select) - See Dynamic RAM (DRAM) Sheet 2, Side A for description of signal.

CAS (Column-Address Strobe) - See Dynamic RAM (DRAM) Sheet 2, Side A.

Microprocessor Circuit



RESET - Instruction to microprocessor stating that either power is initially being applied to PCB or something has gone wrong. During initial powerup RC time constant of resistor R3 and capacitor C20 holds RESET low until +5V stabilizes. During normal operation counter D4 is reset by WDOG Address Decode before D4 reaches count of 8.

16FLIP - See FLIP signal description.

IRQ (Interrupt Request) - Sync-generated signal clocked by microprocessor SYNC output.

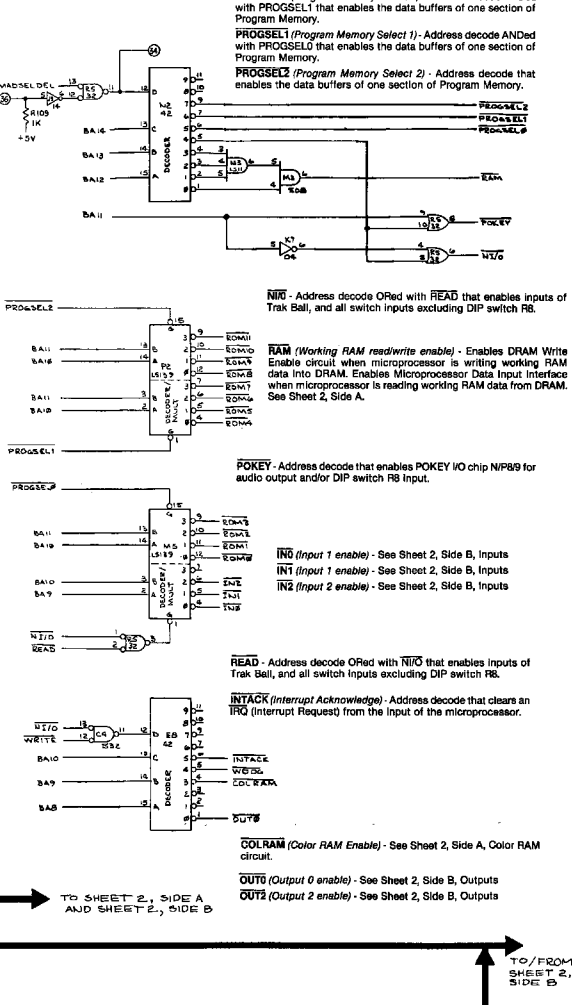
SYNC - Signals generated directly from the microprocessor that indicates the microprocessor is fetching an instruction.

0X (Phase X) - Sync-generated signal equivalent to 2H (1.25 MHz) except during the last 32 scan lines (cites area) of the video display. At this time 0X (0.625 MHz) pulses high on every other high pulse of 2H.

0EXTENDED (Clock Extend) - Microprocessor-generated signal that, when high, delays the 00 clock input (holds 00 high) to the microprocessor while sync is in control of the DRAM during the last 32 scan lines (cites area) of the video display.

00 (Microprocessor clock input) - Sync-generated signal, controlled by the microprocessor and sync, that is the basic clock input to the microprocessor.

Address Decoding



PROGSEL0 (Program Memory Select 0) - Address decode ANDed with PROGSEL1 that enables the data buffers of one section of Program Memory.

PROGSEL1 (Program Memory Select 1) - Address decode ANDed with PROGSEL0 that enables the data buffers of one section of Program Memory.

PROGSEL2 (Program Memory Select 2) - Address decode that enables the data buffers of one section of Program Memory.

TRAK - Address decode ORed with READ that enables inputs of Trak Ball, and all switch inputs excluding DIP switch R8.

RAM (Working RAM readwrite enable) - Enables DRAM Write Enable circuit when microprocessor is writing working RAM data into DRAM. Enables Microprocessor Data Input Interface when microprocessor is reading working RAM data from DRAM. See Sheet 2, Side A.

POKEY - Address decode that enables POKEY I/O chip N199 for audio output and/or DIP switch R8 input.

IN0 (Input 1 enable) - See Sheet 2, Side B, Inputs

IN1 (Input 2 enable) - See Sheet 2, Side B, Inputs

IN2 (Input 3 enable) - See Sheet 2, Side B, Inputs

READ - Address decode ORed with TRAK that enables inputs of Trak Ball, and all switch inputs excluding DIP switch R8.

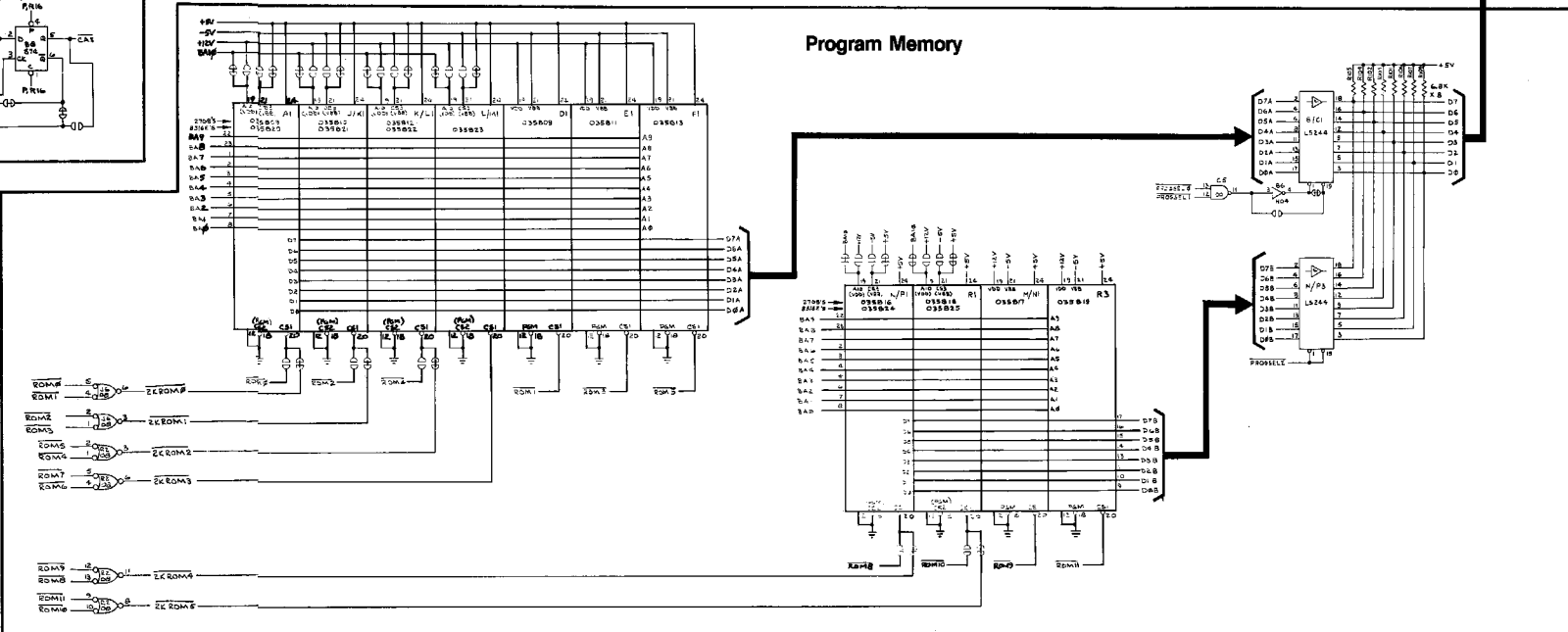
INTACK (Interrupt Acknowledge) - Address decode that clears an IRQ (Interrupt Request) from the input of the microprocessor.

COLRAM (Color RAM Enable) - See Sheet 2, Side A, Color RAM circuit.

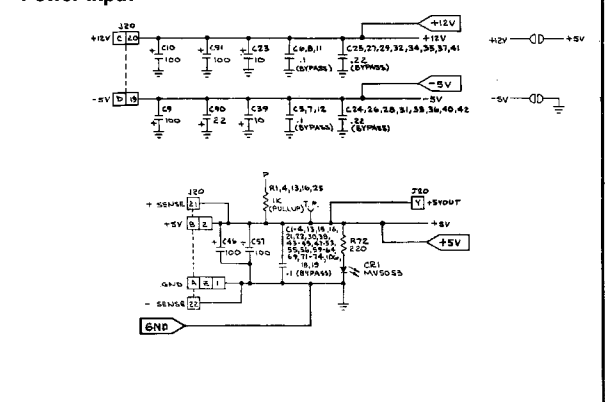
OUT0 (Output 0 enable) - See Sheet 2, Side B, Outputs

OUT1 (Output 2 enable) - See Sheet 2, Side B, Outputs

Program Memory



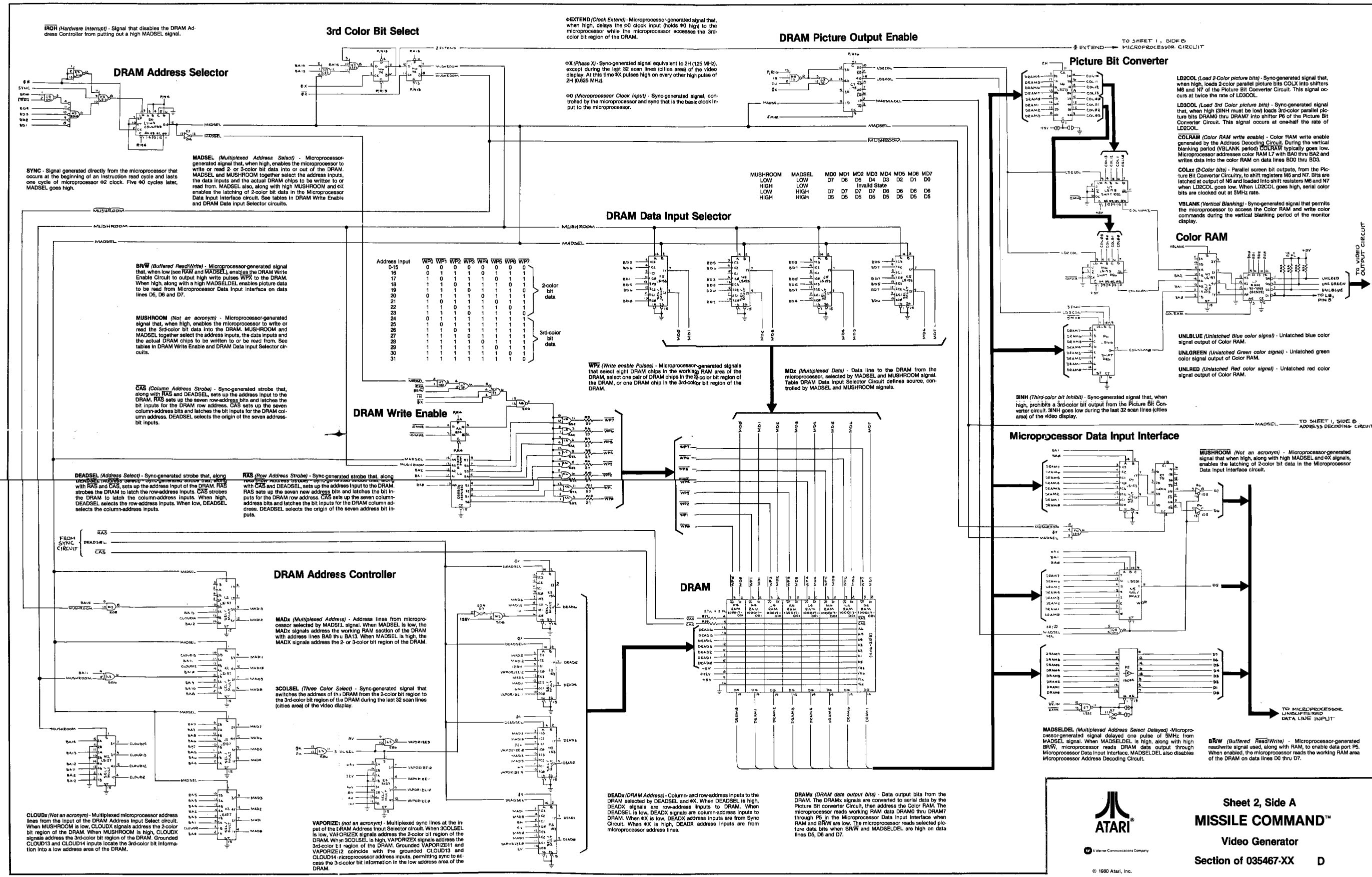
Power Input



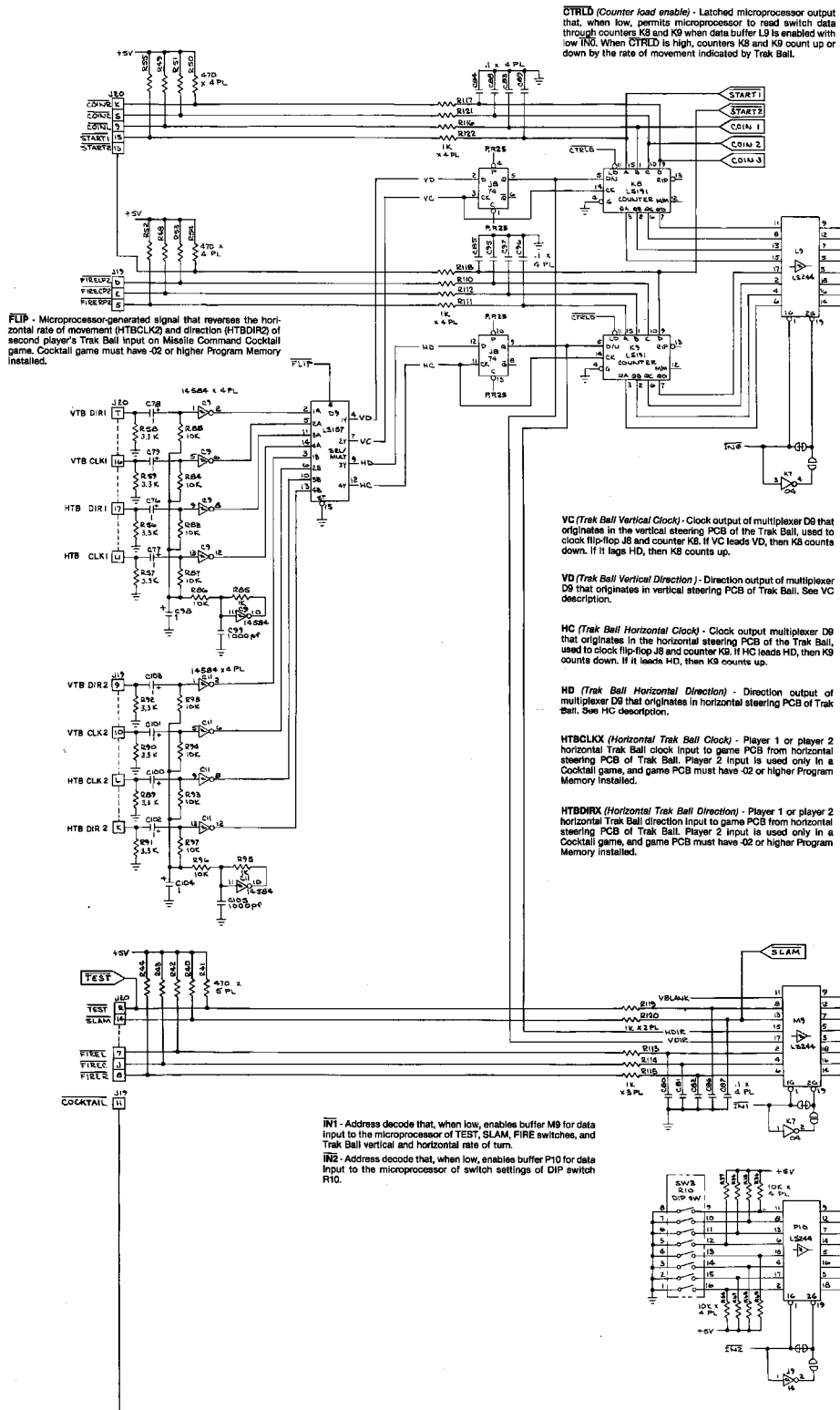
Sheet 1, Side B
MISSILE COMMAND™
 Microprocessor
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Input Circuits



**Memory Map for Address Decoding Circuit,
Sheet 1, Side B**

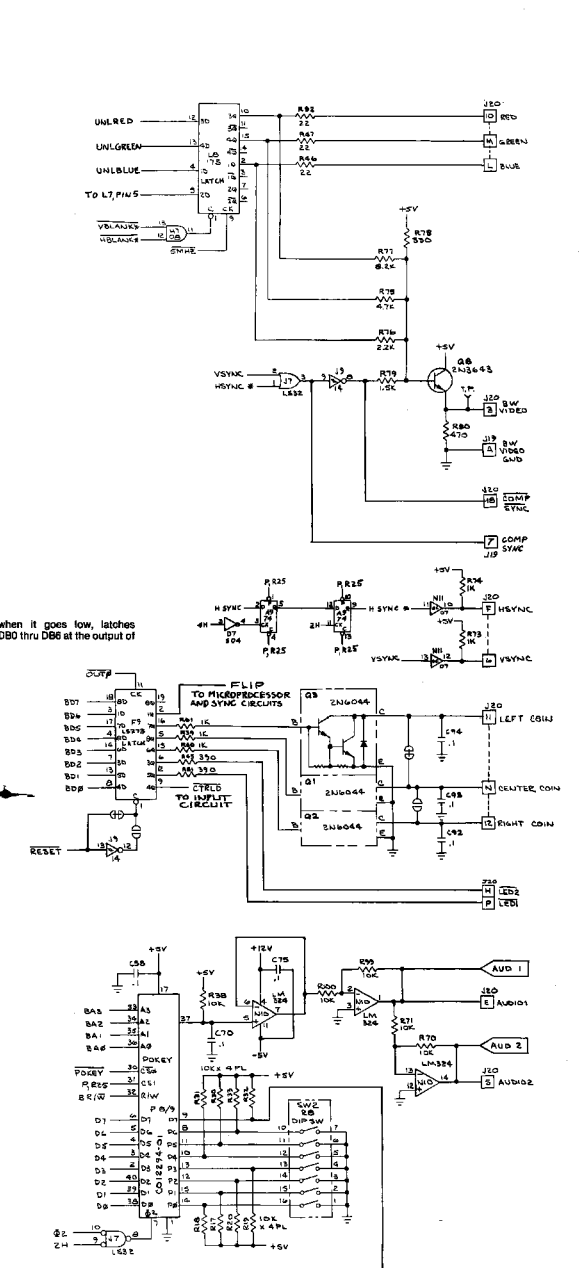
HEXIDECIMAL		ADDRESS																DATA								FUNCTION	
		A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
0000-01FF	0	0	0	0	0	0	0	A	A	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D	512 Bytes of Working RAM	
0200-06FF	0	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D	3rd color-bit region of Screen RAM		
0600-06FF	0	0	0	0	1	1	0	0	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D	More Working RAM		
06FD-3FFF	0	0	A	A	A	A	A	A	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D	2 color-bit region of Screen RAM		
4000-400F	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	POKEY Ports		
4000	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	Right Coin Switch Input		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	Center Coin Switch Input		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	Left Coin Switch Input		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	1-player Start Switch Input		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	2-player Start Switch Input		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	2-player center Fire Switch Input (Cocktail Only)		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	2-player right Fire Switch Input (Cocktail Only)		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	Horizontal TRAK BALL displacement if CTRLD latched High		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	Vertical TRAK BALL displacement if CTRLD latched High		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	Screen Flip		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	Left Coin Counter Output		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	Center Coin Counter Output		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	Right Coin Counter Output		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	2-Player Start LED Output		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	1-Player Start LED Output		
4000	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	CTRLD - If low, read Switches. If high, read TRAK BALL		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	VBLANK read		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	Self-Test Switch Input		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	SLAM Switch Input		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	Horizontal TRAK BALL Direction Input		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	Vertical TRAK BALL Direction Input		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	1st-player left Fire Switch Input		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	1st-player center Fire Switch Input		
4A00	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	Option Switch Inputs		
4B00-4B07	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	Color RAM		
4C00	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	Watchdog		
4D00	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	Interrupt Acknowledge		
5000-7FFF	0	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	Program		

VTB CLKX (Vertical Trak Ball Clock) - Player 1 or player 2 vertical Trak Ball clock input to game PCB from vertical steering PCB of Trak Ball. Player 2 input is used only in Cocktail game, and game PCB must have Q2 or higher Program Memory installed.

VTB DIRX (Vertical Trak Ball Direction) - Player 1 or player 2 vertical Trak Ball direction input to game PCB from vertical steering PCB of Trak Ball. Player 2 input is used only in Cocktail game, and game PCB must have Q2 or higher Program Memory installed.

IN0 - Address decode that, when low, enables buffer L9 for data input to the microprocessor of COIN switches, START switches, player 2 FIRE switches (for Cocktail game only), or Trak Ball rate of turn information. If CTRLD is low, data is from switches. If high, Data is Trak Ball Information.

Output Circuits



Sheet 2, Side B
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