Williams®

16P-3001-300
OCTOBER, 1981

DEFENDER

THEORY OF OPERATION

EARLY SYSTEM BOARDS

- CPU/VIDEO BOARD
  Upright Games Only
- ROM BOARD
  Upright or Table Games
- INTERFACE BOARD
  Upright or Table Games
- POWER SUPPLY
  Upright or Table Games

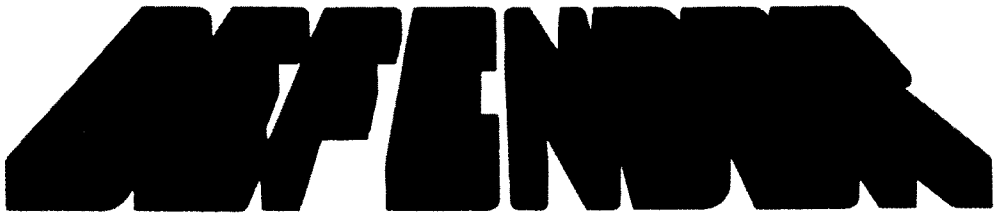
(Refer to 16P-3001-301 for theory on Defender later system boards)

FOR SERVICE...
NOTE NEW TOLL-FREE TELEPHONE NUMBERS:

800-621-1253
IN ILLINOIS CALL:
800-572-1324

Williams® ELECTRONICS, INC.

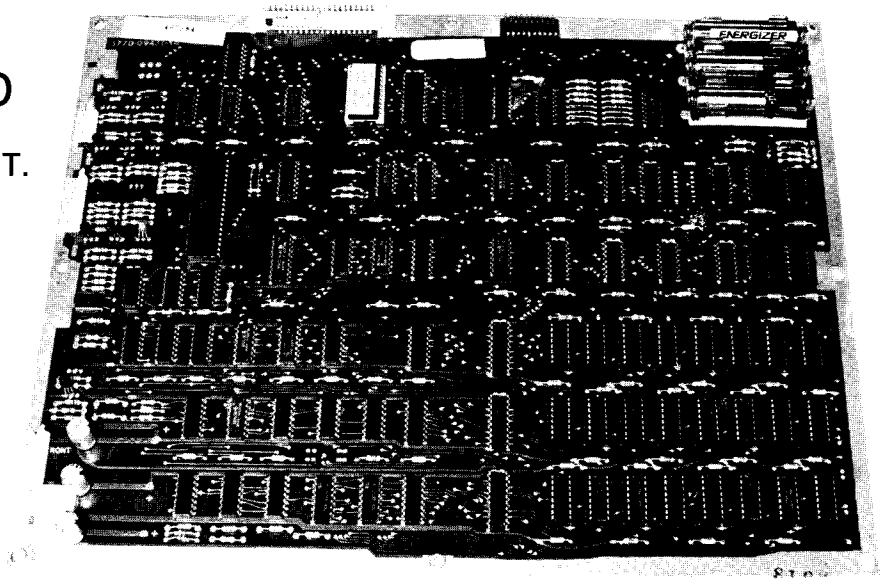
3401 N. California Ave., Chicago, IL 60618
Cable Address: WILCOIN, CHICAGO
(312) 267-2240

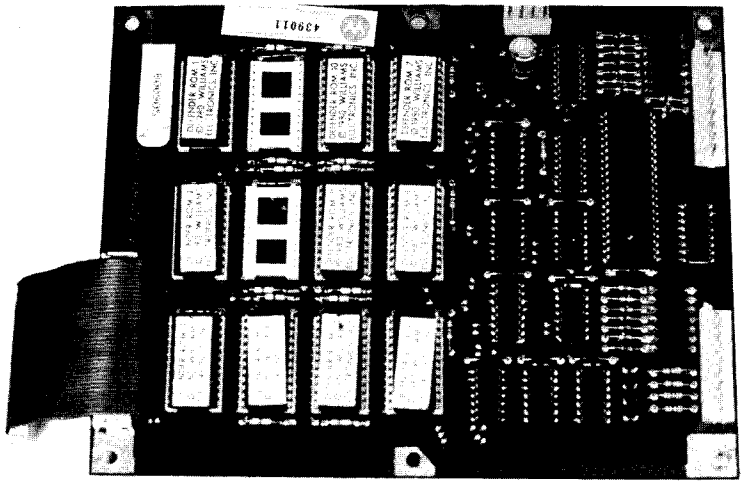


CONTENTS

IDENTIFICATION OF EARLY SYSTEM BOARDS

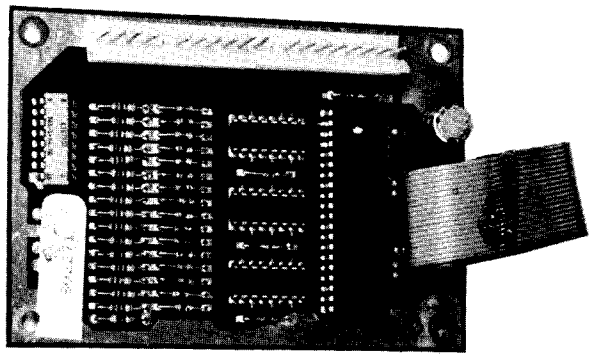
- CPU/VIDEO BOARD
  SINGLE DECODER ROM,
  BATTERIES AT UPPER RIGHT.





- ROM BOARD
  14 AND 16-PIN ICS
  MOUNTED PARALLEL
  TO ROM ICS.

- INTERFACE BOARD
  TOTAL OF FOUR CHIPS
  PLUS RESISTOR PACK.



SECTION 1 INTRODUCTION

The video system in this game consists of five (5) printed circuit boards, a number of switches, and a Video Monitor. The printed circuit boards contain most of the electronic circuitry in the game. Switches provide controlling inputs for play of the game and the Video Monitor provides a high-resolution color display of game action.

The basic functions of the five circuit boards are as follows. (Refer to Figure 1-1.) The Power Supply provides the necessary voltages for proper game operation. Regulated DC outputs of +5VDC, -5VDC, +12VDC, and unregulated DC outputs of +12VDC, -12VDC, and +27 VDC are supplied. An additional AC output (6.3 VAC) is used to power lamps for general illumination purposes.

The CPU/Video board contains a microcomputer Central Processing Unit (CPU), which performs the "brain" function of the system. The CPU controls the rest of the system according to the program (list of instructions) assigned to it by a programmer. This board also contains the Video Control circuitry and Video Memory. The information stored in the Video Memory represents the picture the CPU wants displayed on the Video Monitor. The Video Control circuits read the contents of the Video Memory and convert these contents into color signals which are then fed to the Video Monitor.

The ROM board provides ROM storage for the programs and data base which control the operation of the Video System and supply the necessary data for game operations. The ROM board contains: the game program, the diagnostic (self-test) programs, permanent data used by programs, and I/O (Input/Output) ports. An Input port is used by the system to check the status of input switches. An Output port is used to control the on-board Self-Test indicator LEDs, and game play-selected sounds produced by the Sound Board.

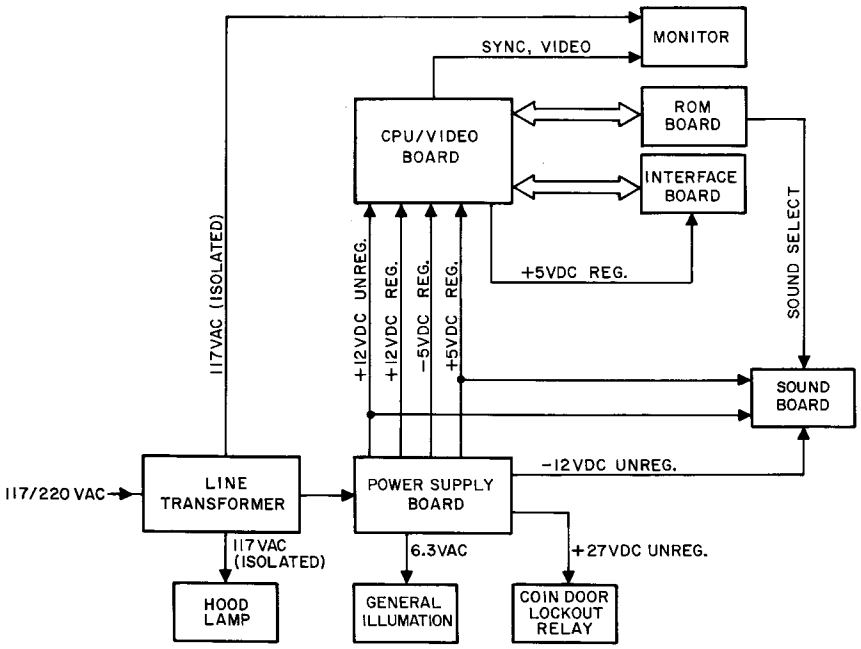


Figure 1-1. Simplified Block Diagram

The Sound Board is able to generate various sound effects upon appropriate command from the CPU. These commands are received via the ROM board. The audio signals generated in response to these commands are amplified on-board, and routed directly to the game speaker system.

The Interface Board provides input ports to interface the Video System to the Player Control Panel. These inputs allow the CPU to check the status of the 1-and 2- player start switches and player panel control switches.

SECTION 2 BLOCK DIAGRAM THEORY

The Williams Video Game System generates a color video display of 360 x 240 pixels (picture elements) on a standard Color Monitor. The Color Monitor provides one complete (non-interlaced) scan of the screen every 16.66 mSec, for a standard frame rate of 60 Hz. The screen may contain up to 16 different colors at once, which are selected under program control from a total of 256 available colors. For each pixel to be displayed, a 4-bit binary code representing one of the 16 currently-available colors is stored in a memory called the Video RAM. These 4-bit pixel codes are continuously read out of the Video RAM in the order they are to be displayed, and used as an address to access 1 of 16 8-bit codes stored in a 16 byte memory called the color RAM. Each of these 16 codes represents 1 of the 256 total available colors (2^8=256). Each 8-bit color code output from the color RAM represents a different combination of brightness levels for the Red, Blue, and Green guns in the monitor, producing 1 of the 256 possible color combinations.

The result is a process of two basic steps for the display of a picture:

1. Select 16 of 256 available colors for the current display by loading the 8-bit value for each color selection into 1 of the 16 color RAM locations. The address at which each color code is stored determines which 4-bit pixel code will cause it to be displayed.

2. Select which of the 16 currently available colors will be displayed at each pixel location on the screen by storing the appropriate 4-bit codes in the Video RAM.

Figure 2-1 is a block diagram showing the main features of the Williams Video Game System hardware.

The Reset circuit produces 2 reset pulses, $\overline{\text{RESET}}$ (Reset Not) and CR (Clocked Reset Not), in response to either a low supply voltage (power-up or power-down) or the reset pushbutton being depressed. These pulses assure that the MPU (Microprocessor Unit) and critical timing components such as the Video Address Generator are forced into a stable state during power fluctuations or testing, and synchronized when normal operation begins. When the reset condition has terminated, a properly functioning MPU will restart the main program, executing system diagnostics and then the game program itself.

The Watchdog circuit is a timer which resets the MPU unless it is cleared before it counts 8 vertical scans. The timer is cleared by writing a specific data pattern at a specific memory address. The command to clear the Watchdog is built into the game program so that during normal game operation the Watchdog is always cleared before it forces the MPU to reset. Should the MPU stop executing the proper instruction sequences and fail to clear the Watchdog, the reset will bring the game up in "Game Over".

The Clock Generator provides basic timing for the video system and consists of a 12 MHz oscillator and dividers to 4 MHz and 6 MHz clocks. The $\overline{12\text{ MHz}}$ clock is also applied to the Video RAM Timing Circuit with other derived timing signals to provide timing for access to the Video RAMs. The $\overline{4\text{ MHz}}$ clock signal derives the E and Q clocks required by the MPU, clocks the Video Address Generator, and, (with the $\overline{6\text{ MHz}}$ clock), provides timing for the Video Shift Registers.

The E and Q Generator divides the $\overline{4\text{ MHz}}$ clock to produce E and Q clocks. These 1 MHz clock phases provide the timing for the MPU and are also applied to the Video RAM Timing Circuit.

The Video Address Generator provides the 14 addresses that scan the Video RAM to produce a frame on the monitor 60 times a second. Function $\overline{CR}$, (Clocked Reset Not), is synchronized with the E clock and holds the counter reset when it is low. When it goes high, the 4 MHz clock is counted to produce the addresses. The addresses are applied through the Video Address Multiplexer to scan the Video RAM banks. In addition, an output is applied to the Watchdog circuit and outputs are decoded to provide horizontal and vertical sync for the Color Monitor and blanking in the Video D-to-A Driver.

The three RAM Banks are scanned simultaneously by the Video Address Bus, and individually by the microprocessor.

The Video RAM Control Circuit accepts microprocessor address bits A8 through A15 to address a PROM. The PROM provides pseudo-address bits PA8 through PA13, and $\overline{E}$ and $\overline{WE}$ (Enable Not and Write Enable Not) functions. This control circuit allows the microprocessor to access the Video RAM Banks individually with sequential addresses. The circuit also provides multiplexing signal MUX 1 to the Video RAM Address Multiplexer.

The Video RAM timing circuit uses the $\overline{12\ MHz}$, E, and Q clocks to produce Video RAM timing. Each Video RAM bank provides 16K address locations, and is accessed with seven address bits at a time. The memory in the RAM is configured in a matrix with 7 of the 14 address bits latched in to select a row in the memory matrix and then the remaining 7 address bits latched in to select a column.

Function $\overline{RAS}$ (Row Address Select Not) and $\overline{CAS}$ (Column Address Select Not) latch the addresses into the RAM at the proper time. Functions MUX 1 from the Video RAM control circuit and MUX 0 pass high, and low-order video address bits for video access, also low-order microprocessor address bits and pseudo-address bits for microprocessor video access.

Function $\overline{SRL}$ (Shift Register Load Not) latches the data outputs from the three RAM Banks into the Video Shift Register after each video access. Function $\overline{WE}$ is produced at an appropriate time during microprocessor access to enable the $\overline{WE}$ (Write Enable Not) outputs from the Video RAM control circuit.

The Video RAM Address Multiplexer uses the MUX 0 and MUX 1 signals to place appropriate addresses on the Memory Address Bus (MAØ through MA6) for latching by the $\overline{RAS}$ and $\overline{CAS}$ signals.

MUX 0	MUX 1	ADDRESSES	RAM
LOW	LOW	UP AD, Pseud.A8-A13	Row
HIGH	LOW	UP A1-A7	Column
LOW	HIGH	VA0-VA6	Row
HIGH	HIGH	VA7-VA13	Column

Video RAM is accessed by the Video Address Bus every microsecond and the data is latched into the Video Shift Register. When the microprocessor reads from RAM, the $\overline{E}$ (Enable Not) signal from the Video RAM control circuit latches the data from the appropriate RAM Bank into the MPU Data Bus.

The Video Shift Registers load the data from the RAM Banks into shift registers. Functions $\overline{SRL}$ (Shift Register Load Not) and the $\overline{4\ MHz}$ clock synchronize loading of data into the shift register. The $\overline{6\ MHz}$ clock shifts out the 4-bit sets of data in parallel. The data loaded into the shift registers in sets of four bits define a pixel (picture element). Four bits from RAM Bank 1 are first presented to the Color RAM Address Multiplexer for a pixel. The next $\overline{6\ MHz}$ clock pulse shifts the other 4 bits from RAM Bank 1. The next two clock pulses shift out

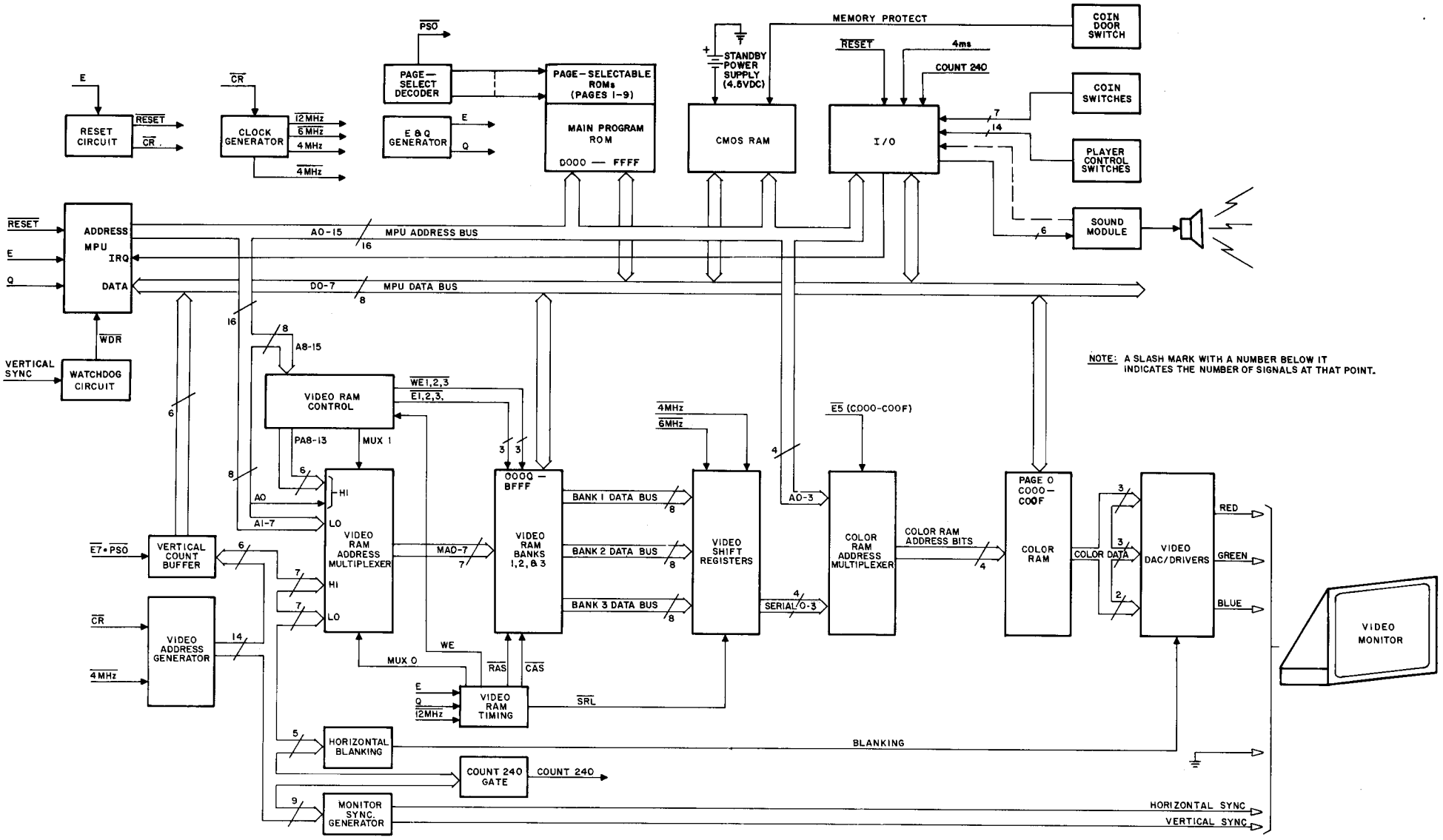


Figure 2-1. Main Features of Williams Video Game System Hardware

the bits from RAM Bank 2 and the third and fourth clock pulses, the bits from RAM Bank 3.

Function $\overline{SRL}$ occurs at a 1 MHz rate, loading sets of four bits into the shift register. The $\overline{6\ MHz}$ clock shifts the sets of bits out prior to the next load.

The Color RAM Address Multiplexer passes 4-bit sets from the Video Shift Registers to the color RAM. The color RAM is a 16 x 8-bit memory addressed by the four bits. Data stored in the color RAM selects a color for a pixel.

The content of the color RAM is set up initially, and changed during the game by the MPU. When the MPU writes to the color RAM, function $\overline{E5}$ (Enable 5 Not) is produced to select MPU address bits A0 through A3 through the address multiplexer, and the state of MPU data bits D0 through D3 are written into the desired color RAM location.

The 8-bit output from the color RAM is applied to the video D-to-A driver. Three bits define seven intensities for the Red gun, three bits for seven intensities of the Green gun, and the remaining two bits for three intensities of the Blue gun.

The Monitor Sync Generator decodes video outputs from the Video Address Bus to produce horizontal and vertical sync pulses for the Color Monitor. The Horizontal Blanking circuit also decodes Video Address Bus outputs to blank the Color Monitor at the left and right edges of the screen. The Video RAM corresponding to these areas are available to the MPU for "scratchpad" RAM, and the horizontal blanking overlaps the internal Color Monitor horizontal retrace blanking to prevent display on the Color Monitor.

The program is able to determine the vertical position of the scan on the screen at any time by reading the Vertical Count Buffer. Function $\overline{E7}\cdot\overline{PS\emptyset}$ (Enable 7 Not AND Page Select 0 Not) latch the higher order Video Address Bus bits onto the MPU data bus for reading.

In addition, when the trace reaches the bottom of the screen, count 240 is decoded from the Video Address Bus and applied to an I/O (Input/Output) port on the ROM Board to produce an MPU Interrupt. Also, Video Address Bit A11 is applied to the I/O port on the ROM Board to produce a 4 mSec Interrupt.

The Page 0 decoder is provided with Page 0 select functions from the ROM Board and MPU Address leads and enables MPU access to the Interface Board I/O, the Vertical Count Buffer, CMOS RAM, and the color RAM. The MPU reads and writes to the Interface Board and CMOS RAM, reads the Vertical Count Buffer, and writes to the color RAM.

The CMOS RAM is provided with standby battery power to maintain audit information and game adjustments. The CMOS RAM provides 256 4-bit memory locations. Audit information stored in the lower half of the memory, is written to as a part of game operation, and is read from as part of the high score signature attract mode. Game adjustments are stored in the upper half, and during game operation are only read. A "memory protect" switch is held closed when the coin door is closed to provide the Memory Protect function. This prevents writing to the upper half of the memory when the coin door is closed. With the coin door open, writing to the upper half is allowed so that changes to adjustments can be made.

Pages are selected by writing to $D\emptyset\emptyset\emptyset_{16}$ with data to select one of up to 1Ø pages. Address decoding provides chip-selects for the ROMs, for the inputs, and PIA.

The ROM Board PIA scans coin door switches and provides outputs to the Sound Board. This PIA also provides outputs for the diagnostic LEDs. The 4 mSec and Count 24Ø functions from the CPU/Video Board produce interrupts to the MPU.

The Model Interface Board accepts inputs from player panel switches through a PIA. The Page Ø Decoder on the CPU/Video Board provides a select-input for the PIA.

SECTION 3 DETAILED THEORY

RESET CIRCUIT (Figure 3-1)
The Reset Circuit ensures orderly start-up and recovery of the game by forcing a reset in response to any of the following situations:

1. Power-up (Unit is turned on or power failure has ended).
2. Power-down (Unit is turned off or power failure has occurred).
3. Reset pushbutton on CPU/Video board is depressed.
4. Low line or power supply voltage.

A Reset causes the MPU to start at the proper memory location, disables the CMOS RAM until the MPU is stable, forces all PIA ports to inputs, and synchronizes both the Video Address Generator and the 6MHz clock with the E clock.

Two signals are used for the Reset function: $\overline{\text{RESET}}$ (Reset Not), and $\overline{\text{CR}}$ (Clocked Reset Not). The $\overline{\text{RESET}}$ pulse width (approximately 1 second) is determined by the RC time constant R2/C1. $\overline{\text{CR}}$ is clocked high after $\overline{\text{RESET}}$ goes high by the next rising edge of the E clock, ensuring that the Video Address Generator and 6MHz divider are synchronized with the E clock when $\overline{\text{CR}}$ goes high.

When power is applied, C1 begins to charge through R2. At this point transistors Q4, Q5, Q1, & Q2 are all off. This allows R10 to pull $\overline{\text{RESET}}$ low, asserting the reset function. Since the $\overline{\text{CL}}$ (Clear Not) input of the data latch which generates $\overline{\text{CR}}$ is tied to $\overline{\text{RESET}}$, its Q output is forced low, asserting $\overline{\text{CR}}$.

As the charge on C1 reaches approximately 0.9 VDC, Q1 is biased on through R1 and R3. This has no immediate effect, but enables Q2, which will be turned on later. C1 continues to charge, and at approximately 3.0 VDC biases on Q4. As Q4 begins to conduct, it pulls its collector current through R4 and R6, increasing the voltage drop across these resistors. When the voltage drop across R6 increases to 0.7 VDC, Q5 is biased on and starts to pull $\overline{\text{RESET}}$ toward +5 VDC.

Since Q1 was turned on earlier, there is a current path to ground from the emitter of Q2, causing Q2 to turn on as the voltage on $\overline{\text{RESET}}$ rises. Once Q2 turns on, its collector draws current through R17, increasing the base current of Q5. At this point Q2 and Q5 continue to increase each other's base drive until both transistors are saturated, latching each other in this condition. The purpose

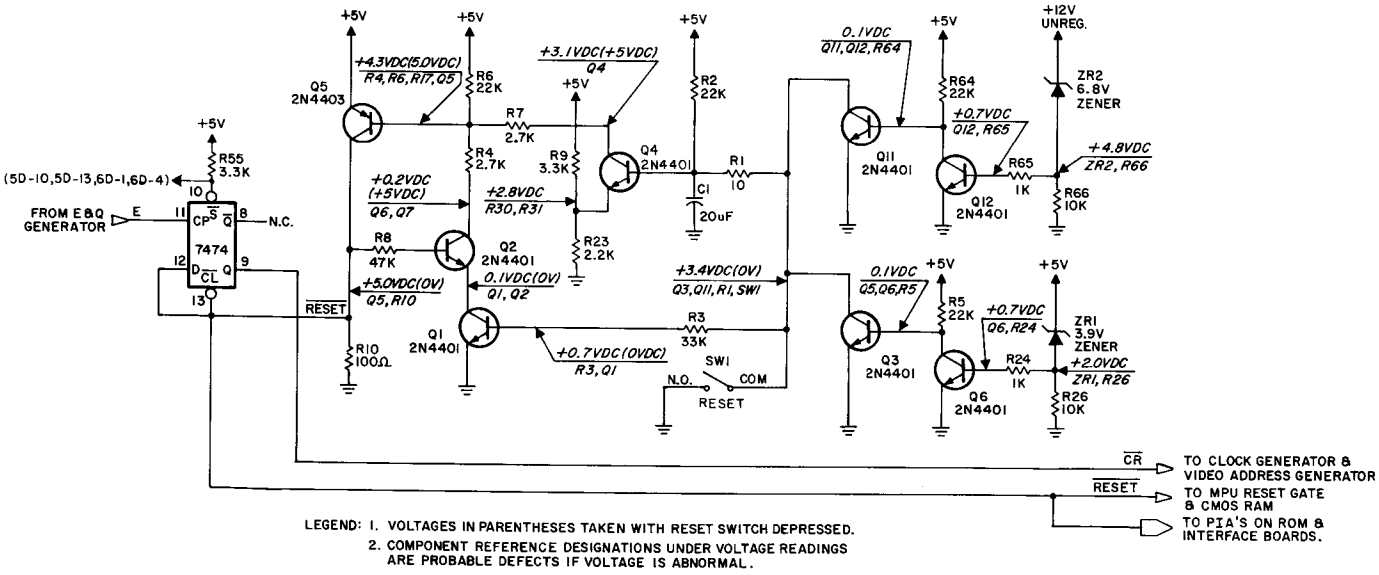


Figure 3-1. Reset Circuit

of this latch is to provide a fast transition of $\overline{\text{RESET}}$ from its asserted (low) state to its negated (high) state.

With $\overline{\text{RESET}}$ high, $\overline{\text{CR}}$ will go high at the next rising edge of E clock, which clocks the high present at the D input of the data latch out to the Q output.

Depressing Reset switch, SW1, shorts the charge on C1 to ground. This turns off both Q1 and Q4. When Q1 turns off it breaks the emitter circuit of Q2, forcing it off and breaking the Q2/Q5 latch effect. Since neither Q2 or Q4 is supplying base drive to Q5, it turns off, allowing $\overline{\text{RESET}}$ to be pulled low by R10, forcing $\overline{\text{CR}}$ low. When the Reset button is released, C1 begins to charge again. From this point, the circuit operates as described in the power-up sequence.

The power-down sequence is triggered by either the +12 VDC unregulated supply or the +5 VDC regulated supply dropping below acceptable limits. Since the operation of the sensing circuits is similar, only the +12 VDC sensor is described.

During normal circuit operation, ZR2 is biased on, but is operated close to its turn-off point by R66. Some of the current flowing through ZR2 also flows through R65, biasing Q12 on. The collector of Q12 pulls the base of Q11 down to 0.1 VDC, forcing Q11 off.

When a power-down (or voltage drop) occurs, ZR2 stops conducting as the supply voltage drops. This removes the base bias of Q12, turning it off and allowing R64 to bias Q11 back on. This has the same effect as pushing the RESET button, shorting the charge on C1 to ground, thereby asserting reset outputs $\overline{\text{RESET}}$ and $\overline{\text{CR}}$.

WATCHDOG CIRCUIT (Figure 3-2)

The Watchdog Circuit is a timer which resets the MPU if it is not cleared at least once every 133 mSec. To clear the watchdog timer, the MPU writes a specific data byte (38_{16} or 39_{16}) into address $C3FF_{16}$ with page 0 selected. The game program is designed to perform this clear operation regularly, ensuring that the watchdog will not reset the MPU during normal operation.

Noise transients and other problems will sometimes cause an MPU to jump out of the normal program sequence. If this happens the MPU will often misinterpret

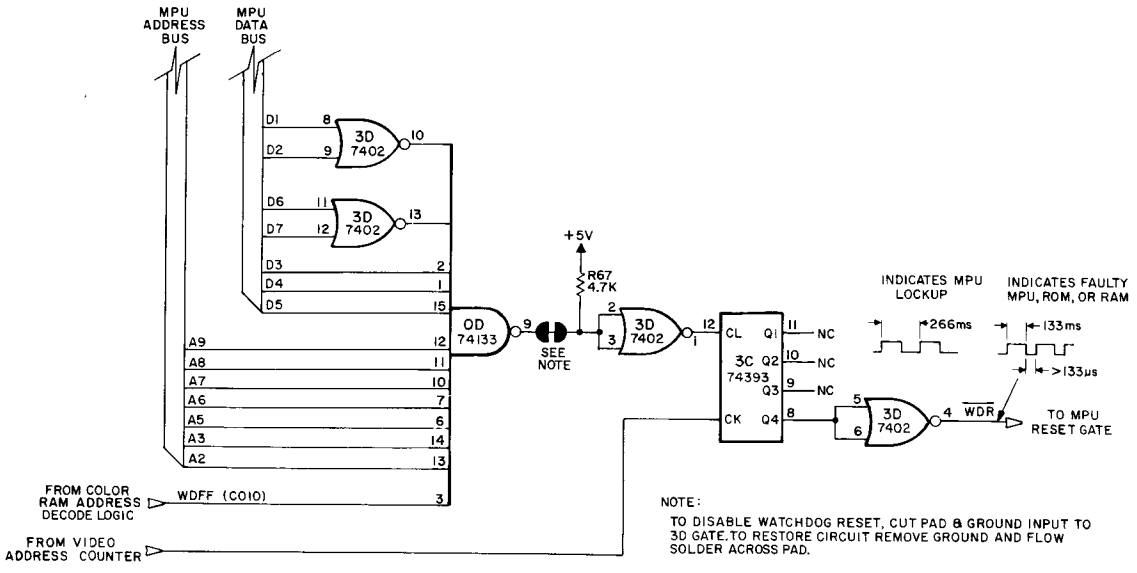


Figure 3-2. Watchdog Circuit

instructions and data, causing it to become stuck in a continuous program loop which has nothing to do with the real intent of the program. Because it is "caught in a loop", the MPU will not clear the watchdog timer, and after 133 mSec, the watchdog circuit issues a $\overline{WDR}$ (Watchdog Reset Not) pulse to the MPU reset gate. The MPU is forced to reset and begin proper program execution.

Function WDFF (Watchdog Flip-Flop) from the color RAM address decode logic is gated with the MPU Address and Data bits as shown.
The output of gate ØD goes low when the MPU writes 38_{16} or 34_{16} into address $C3FF_{16}$ with Page 0 selected. This signal is inverted to clear the Watchdog timer 3C. The timer counts vertical scans from the Video Address Generator Circuit parallel-load pulse at inverter IJ pin 10. If the counter is allowed to count eight vertical scans (133 mSec) without being cleared, its Q4 output will go high, causing $\overline{WDR}$ to go low, to force an MPU reset.

Note that there is a special pad shown which may be broken, and one side grounded in order to disable the Watchdog circuit. This may be necessary to troubleshoot certain problems if the Watchdog circuit repeatedly resets the MPU.

MPU (Figure 3-3)
The MPU (Microprocessor Unit) address and data busses, and the R/$\overline{W}$ (Read/Write Not) control signal are buffered because the number of devices loading them would exceed the drive capability of the MPU chip.

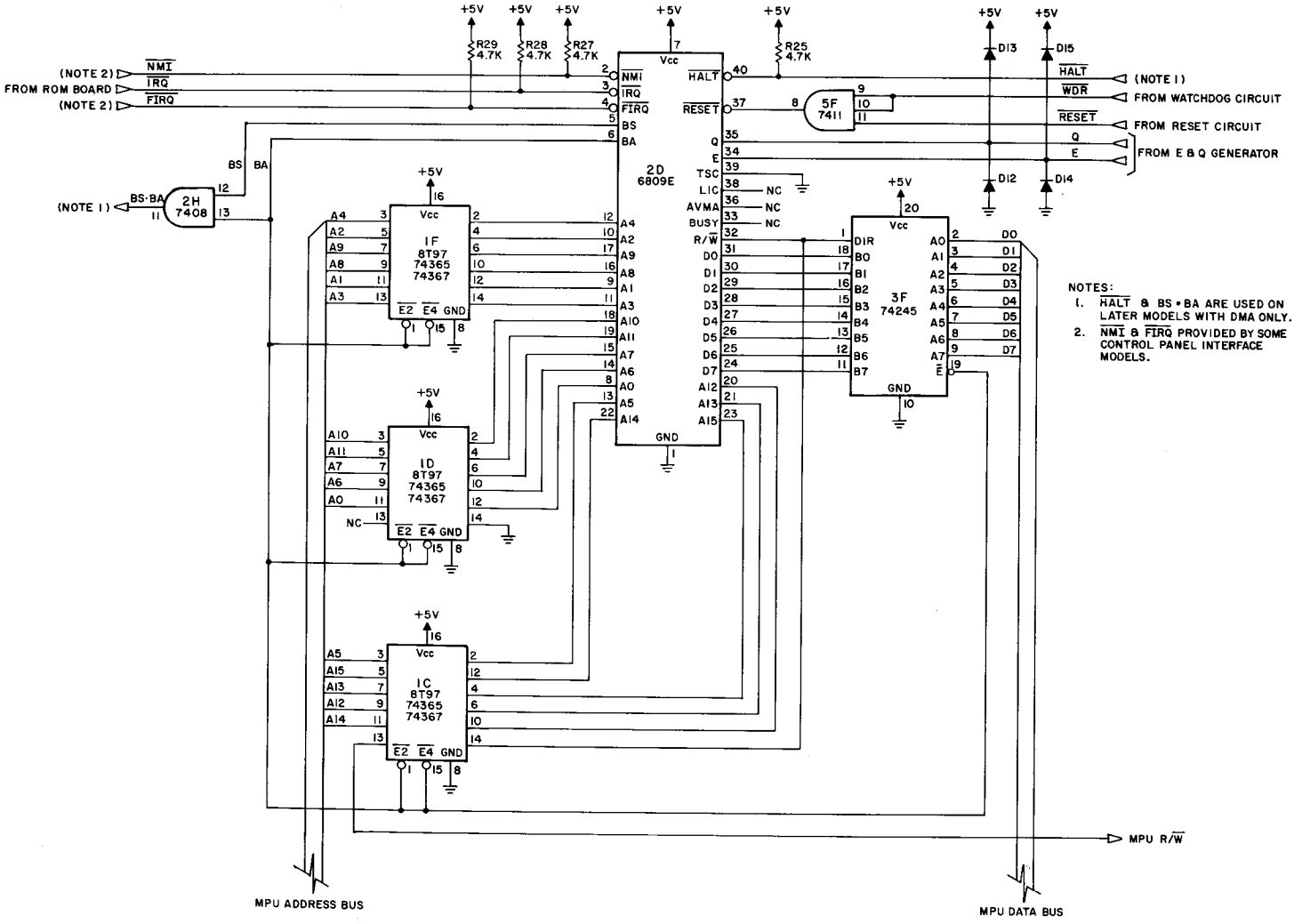


Figure 3-3. MPU

The buffers driving the address and R/$\overline{W}$ lines are uni-directional, transmitting signals from the MPU outputs to the bus. The data bus buffers are bi-directional, transmitting data from the bus to the MPU when R/$\overline{W}$ is high, and from the MPU to the data bus when R/$\overline{W}$ is low. R/$\overline{W}$ is also used by memory devices and other peripheral devices during data transfers.

During normal operation the buffers are continuously enabled. When a DMA (Direct Memory Access) controller is used, (on later games), the MPU may allow it to drive the busses and R/$\overline{W}$ control line by asserting BA. This disables the buffers, effectively disconnecting the MPU from the address and data busses, and R/$\overline{W}$. The DMA device is then notified by signal BS•BA that it may use the busses.

Four inputs to the MPU ($\overline{HALT}$, $\overline{NMI}$, $\overline{IRQ}$, $\overline{FIRQ}$) are pulled high by resistors (R25, R27, R28, & R29) to ensure that they are not active unless pulled low by a peripheral device. A low on the $\overline{HALT}$ input causes the MPU to enter a halt state, disable its bus buffers and allow the busses to be controlled by another device. At this point BA and BS are asserted: (BA•BS). As stated above, this output is used on later games with a DMA controller.

$\overline{NMI}$; $\overline{FIRQ}$; and $\overline{IRQ}$ are interrupt inputs. Asserting any of these signals causes the MPU to finish its current instruction, save the status of the program being executed, and execute an interrupt service routine. $\overline{NMI}$ and $\overline{FIRQ}$ are not used in early-model games. $\overline{IRQ}$ is supplied by the $\overline{IRQA}$ and $\overline{IRQB}$ outputs (4 mSec and Count 240 interrupt respectively) of the ROM board PIA.

The E and Q inputs to the MPU are both 4 MHz clock signals, with the Q leading E by 90°. A timing diagram of these signals may be found in the E and Q Generator paragraph. Clamping diodes D12 through D15 prevent the MPU E and Q inputs from being driven more than 0.7 VDC above +5VDC or below ground. The MPU reset gate (5F) allows the MPU to be reset by either $\overline{WDR}$ or $\overline{RESET}$.

CLOCK GENERATOR (Figure 3-4)

The Clock Generator Circuit provides three basic clock frequencies from which all system timing is derived. The 12 MHz clock is divided by two to obtain a 6 MHz clock, and by three to obtain a 4 MHz clock.

The 12 Mhz source is a two-inverter crystal oscillator with a third inverter to buffer its output. It is inverted once more to become $\overline{12\ MHz}$ for the Video RAM timing circuit, and $\overline{12\ MHz}$ is then inverted to provide a delayed 12 MHz clock for a latch section of 4B.

The 4B latch supplying 6 MHz is connected in the toggle mode, with the D input driven by the $\overline{Q}$ output. The output (6 MHz) changes states on the rising edge of the 12 MHz clock, providing an output of one half the clock pulse input frequency. The $\overline{S}$ input is driven by $\overline{CR}$, forcing $\overline{Q}$ to a logic zero as long as $\overline{CR}$ is low. $\overline{CR}$ goes high in synchronization with the E clock signal. The 6 MHz output always starts from a logic zero and is in sync with the E clock.

Two JK flip-flops (4C) are configured as a divide-by-three counter. Since the K inputs are tied high, the flip-flops toggle when the J input is high during a high clock pulse. If the J input is low during the clock pulse the flip-flop will perform a clear operation ($\overline{Q}$ = 0, Q = 1). With the J inputs wired to $\overline{Q}$ and Q outputs as shown, the circuit has 3 stable states as shown in the timing diagram. The output pulse rate is an asymmetrical 4 MHz.

To obtain a 50% duty-cycle, the pulse at 4C-6 is used to clear a D latch section of 4B. The rising edge of 12 MHz following this pulse clocks the high at the D input to the Q output, producing a 4 MHz, 50% duty-cycle clock as shown in the

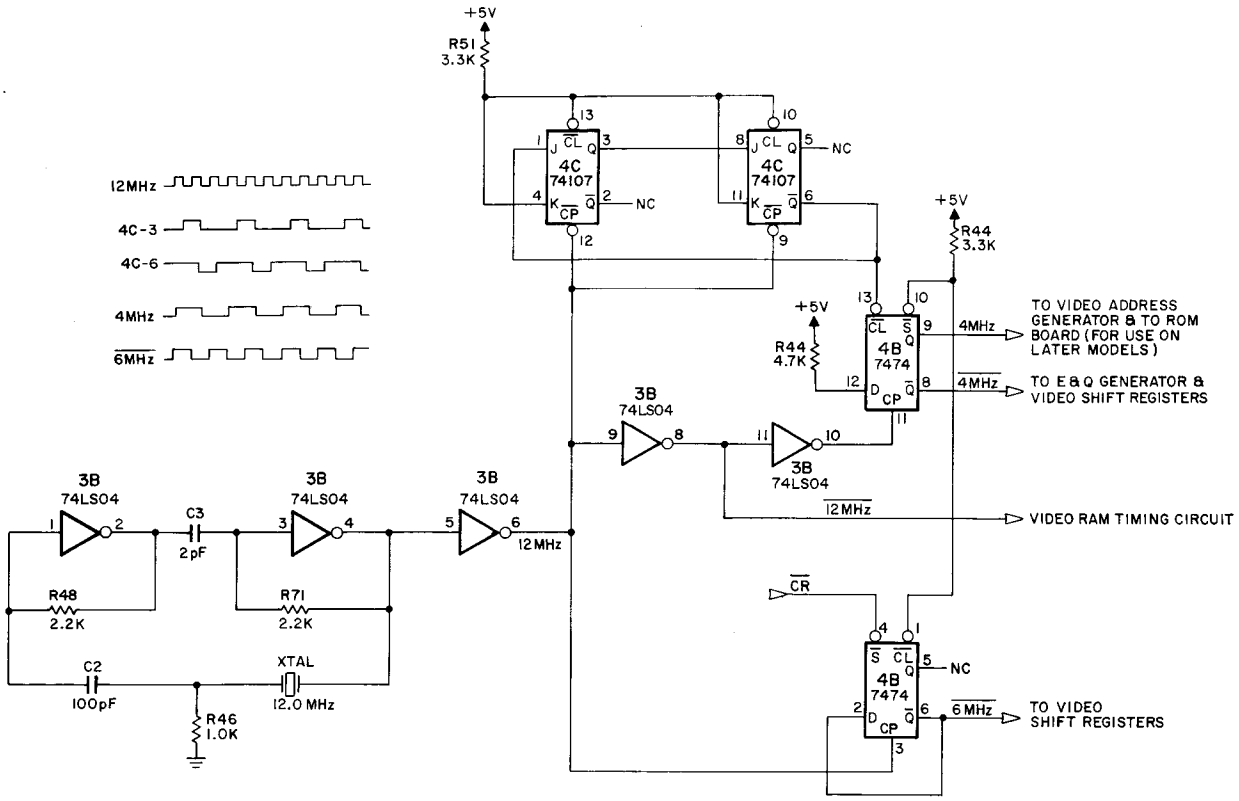


Figure 3-4. Clock Generator

timing diagram. The $\overline{Q}$ output provides a 4 MHz signal which is 180° out of phase with the Q output. Note that the 12 Mhz clock used here is delayed to compensate for the propagation delay of the 4C flip-flops.

E AND Q GENERATOR (Figure 3-5)

The E & Q Generator supplies two overlapping clock signals necessary to the operation of the MPU. These clocks are called E and Q. They are both 1 MHz, 50% duty-cycle, and Q leads E by 90° (250 nSec). Since the MPU accesses memory only when the E clock is high, E is also used by some of the memory decoding circuits, the Video RAM timing circuit, and synchronizes the 6 MHz clock and the Video Address generator.

The E and Q Generator consists of three D-type latches. The first flip-flop has its $\overline{Q}$ output wired to its D input causing it to toggle on the rising edge of the 4 MHz clock. The first flip-flop is wired in the toggle mode with its D input tied to its Q output. This produces a 2 MHz output at the Q and $\overline{Q}$ terminals of this flip-flip. The 2 MHz signal clocks a second flip-flop, also wired in the toggle mode, causing a 1 MHz square wave to appear at its Q output. This is the Q clock signal.

The third flip-flop has its D input tied to the Q clock signal, causing its Q output (the E clock signal) to follow the Q clock. Because this flip-flop is clocked by the 2 MHz signal, it is clocked 90° later than the flip-flop providing the Q clock, causing E to lag Q by 90°. See the timing diagram in Figure 3-5.

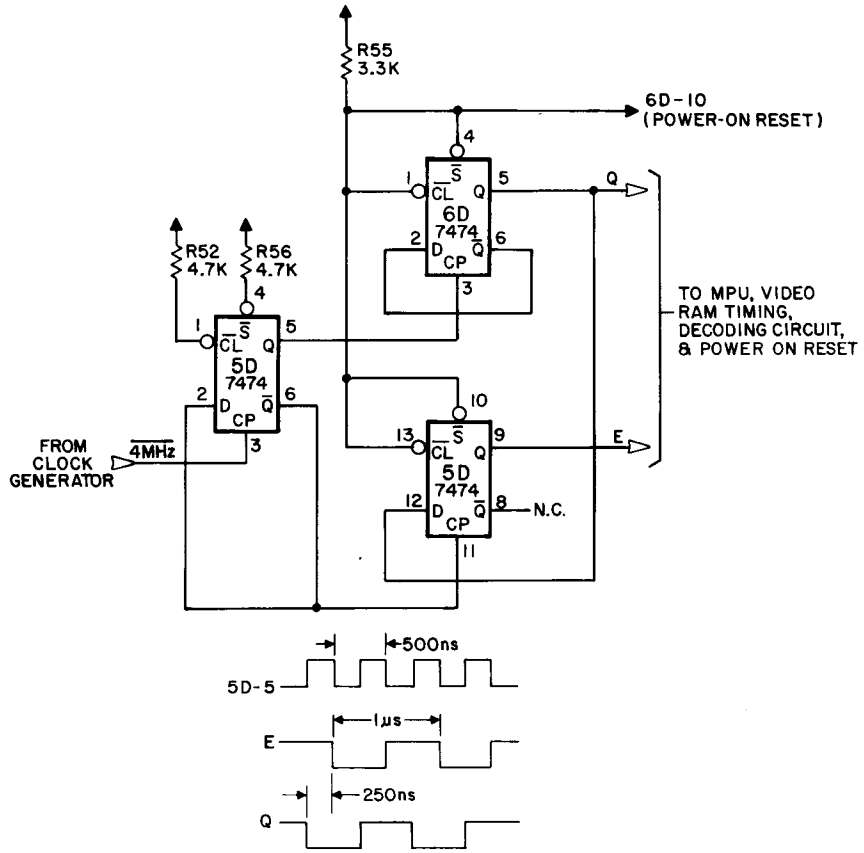


Figure 3-5. E AND Q GENERATOR

Video Address Generator (Figure 3-6)

The Video Address Generator supplies the 14 address-bit which scans the entire Video RAM 60 times each second, reading out pixel codes to the Video Shift Registers. When power is first applied to the system, the Reset circuit asserts $\overline{CR}$ (Clocked Reset Not), clearing the four 9316 type counters (2L, 2N, 20, and 2Q) which generate the Video Address. Function $\overline{CR}$ is synchronized with the 1 MHz E clock. The generator is a 16-bit binary counter with the most-significant 14 bits used as the Video Address bus. The two least-significant bits of the counter generate a carry to VA0 once every 4 counts of the 4 MHz clock, causing VA0 to toggle at a 1 MHz rate, hence incrementing (adding 1 to) the video address once every microsecond.

The least-significant 4-bit counter stage (IC-2L) is continuously enabled by pulling its CEP and CET inputs high, allowing it to count the 4 MHz clock whenever $\overline{CR}$ is high. The parallel inputs for preloading the counter are not used and are grounded. The $\overline{PE}$ input is disabled by tying it high. When this first state reaches its terminal count (all Q outputs high), output TC enables the CEP inputs of the three most-significant counter stages. The CET input of the second 4-bit stage (2N) is pulled high, allowing it to count a 4 MHz clock pulse every time the TC output of the first stage is high. (A high TC output indicates a carry from that stage on the next clock pulse). The second and third 4-bit stages (2N and 20) enable the CET inputs of the next stages in the same manner, causing each stage to count only on a carry from the previous stage, and since all stages are clocked by the same 4 MHz signal, all outputs change on the same clock pulse.

When the last video address ($16,383_{10}$) is reached, all pixel codes in the Video RAM have been read out to the screen, and the Video Address Generator is ready to reset to count 0 on the next clock pulse. Since the video address is incremented once per microsecond, the elapsed time from video address zero to video address $16,383_{10}$ is approximately 16.4 mSec.

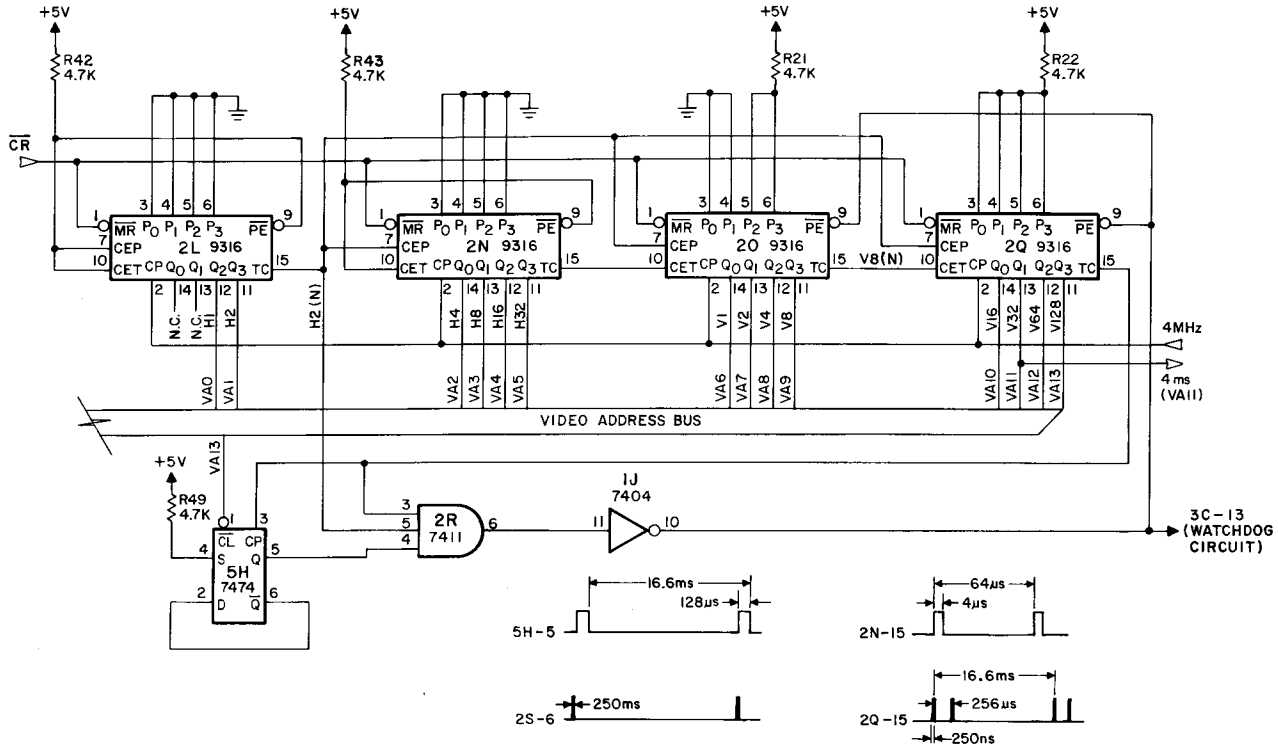


Figure 3-6. Video Address Generator

At this count, the TC output from stage 2Q latches a high at the 5H output. This is gated with the TC outputs from stages 2L and 2Q to produce a low to the PE inputs of stages 2O and 2Q. The next clock pulse preloads these counters to $16{,}128_{10}$ and counting, continuing until $16{,}383_{10}$ is reached a second time, increases the counting time to approximately 16.6 mSec.

When TC from 2Q goes high the second time, a low is latched at the output of 5H. The following clock pulse advances the counter to all zeroes. The $\overline{CL}$ input of the latch is connected to VA13, and as VA13 goes low, the latch (5H) is cleared to provide a parallel load at the next full count.

VIDEO RAM CONTROL (Figure 3-7)

The Video RAM Control Circuit allows sequential MPU addressing of the three 10K video RAM banks. With eight low-order MPU Address Bus bits applied to the RAM, the high-order bits access a PROM for generation of psuedo-address bus and bank-enable signals.

MPU adddress bits A8 through A15 are applied to decoder PROM 1G and appropriate PA8 through PA13 (Pseudo-Address) bits are produced at the D0 through D5 outputs. Bits D6 and D7 provide a bank-select code. MPU Address bits A14 and A15 are gated to produce a low enable function for all addresses below C000. (For addresses C000 through FFFF, both A14 and A15 are high and MPU access to the RAM is inhibited).

With both the D6 and D7 PROM outputs low, 1-of-4 decoder 2F produces a low $\overline{Y0}$ enable signal for RAM Bank 1. A high D6 and low D7 produce a low $\overline{Y1}$ enable signal for RAM Bank 2; A low D6 and high D7 produce a low $\overline{Y2}$ enable for RAM Bank 3. The case of both bits high producing a low $\overline{SMC}$ (Special Multiplex Control Not) is not implemented in the system.

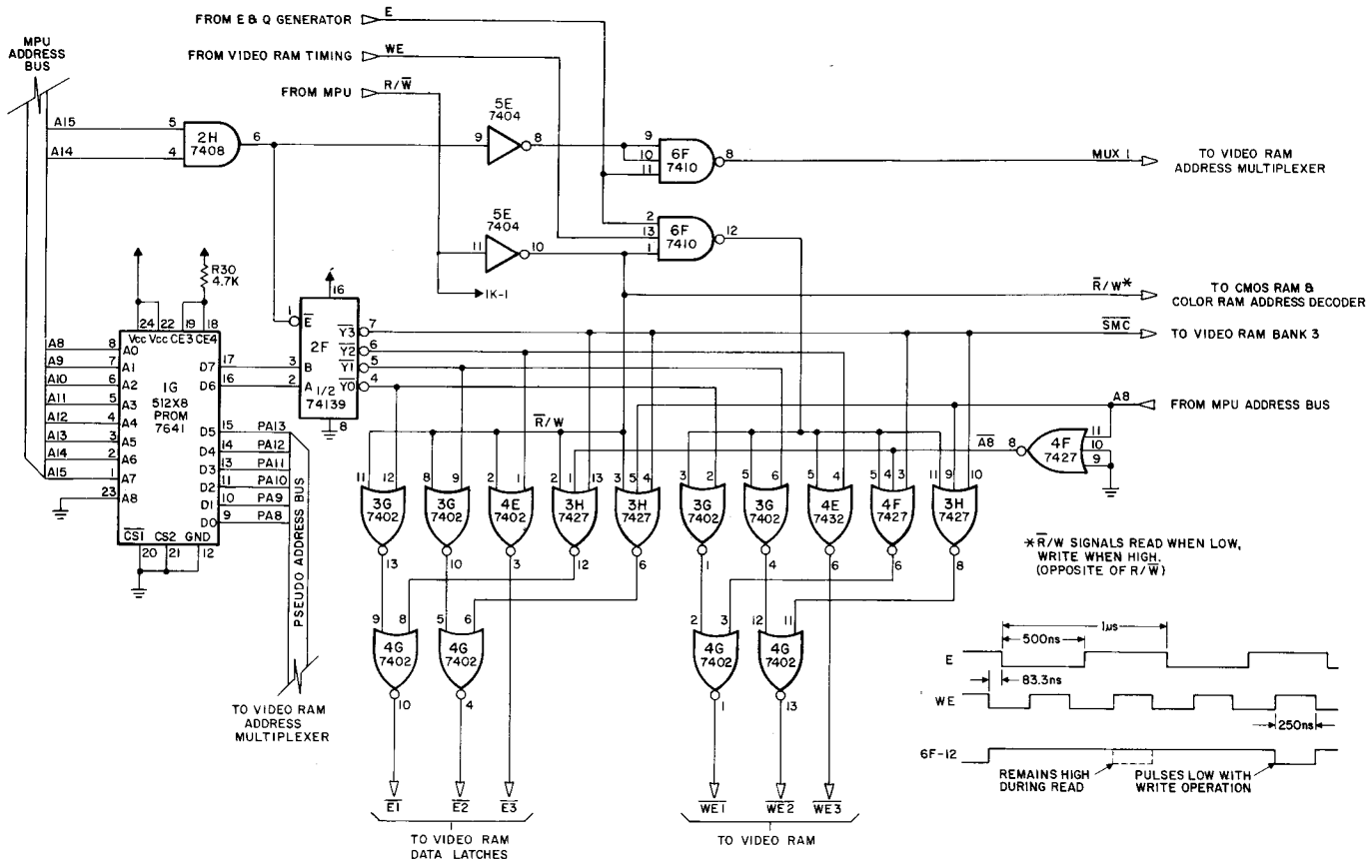


Figure 3-7. Video RAM Control

Function R/$\overline{W}$ (Read/Write Not) is inverted to produce a low during read which is gated with the $\overline{Y0}$, $\overline{Y1}$, and $\overline{Y2}$ functions. This pulses $\overline{E1}$, $\overline{E2}$ and $\overline{E3}$ low, to enable Video RAM data latches for Banks 1, 2, and 3. With a write operation, $\overline{R}$/W (Read Not/Write) is gated with the E Clock and WE (Write Enable) from the Video RAM Timing Circuit to produce a low from 6F pin 12. The E Clock ensures that the function is in phase with the MPU and WE synchronizes the function to the Video RAM access timing. The low output is gated with the $\overline{Y0}$, $\overline{Y1}$ and $\overline{Y2}$ lows to produce low $\overline{WE1}$, $\overline{WE2}$, and $\overline{WE3}$ (Write Enable Not) to enable writing to the three RAM Banks.

NOTE

The 3H and 4F gates connected to the $\overline{Y3}$ output are associated with SMC and provide low outputs at all times (since $\overline{SMC}$ is not used in the system). This causes the 4G gates to effectively serve as inverters for the $\overline{E1}$, $\overline{E2}$, $\overline{WE1}$, and $\overline{WE2}$ enables. Also, since the previously mentioned 3H and 4F gates are locked in a low-output state because of the $\overline{Y3}$ ($\overline{SMC}$) input, the A8 and $\overline{A8}$ inputs have no effect.

The E Clock is gated to produce a low MUX 1 (Multiplex 1) enabling MPU RAM access. For addresses from C000 to FFFF, A14 and A15 inhibit MUX 1. The inverted $\overline{R}$/W function is applied to the CMOS RAM and to the Color RAM Address Decoder.

VIDEO RAM TIMING (Figure 3-8)

The Video RAM Timing Circuit uses the $\overline{12\ MHz}$ and E and Q clocks to produce the timing required for access to the Video RAM. The timing for multiplexing seven memory address bits at a time and latching them into the RAMs is required. In addition, a load pulse is produced every microsecond for shift registers that forward video information toward the Color Monitor.

The E and Q clocks are applied to Exclusive-OR gate 4D; which provides a high output when one, and only one, input is high. A low output occurs if both inputs are high or both are low. The result is a 2 MHz square wave that is clocked into a 3K data latch section at 12 MHz. The $\overline{Q}$ output is then clocked into the second 3K latch section to provide the 2 MHz MUX 0 signal. Clocking through the latches provides the phase relationship needed to multiplex the 14 video address bits into two groups of seven memory address bits for RAM rows and columns (and MPU/Pseudo-Address bits into two groups). When MUX 0 is low, row address bits are selected; when it is high, column address bits are selected.

NOTE

MUX 0 is used in conjunction with MUX 1 from the Video RAM Control Circuit. When the MPU is addressing the RAM any address below C000, and during the high state of the E clock, MUX 1 is low, selecting the two groups of MPU and pseudo-address bits. When the E clock is low, MUX 1 is high, selecting the two groups of video address bits. When the MPU is accessing memory locations from C000 through FFFF, MUX 1 is high, regardless of the state of the E clock. During such MPU cycles, video address bits are selected and the RAM is accessed; however, the data read from the RAMs remains isolated from the video shift register and the MPU data bus.

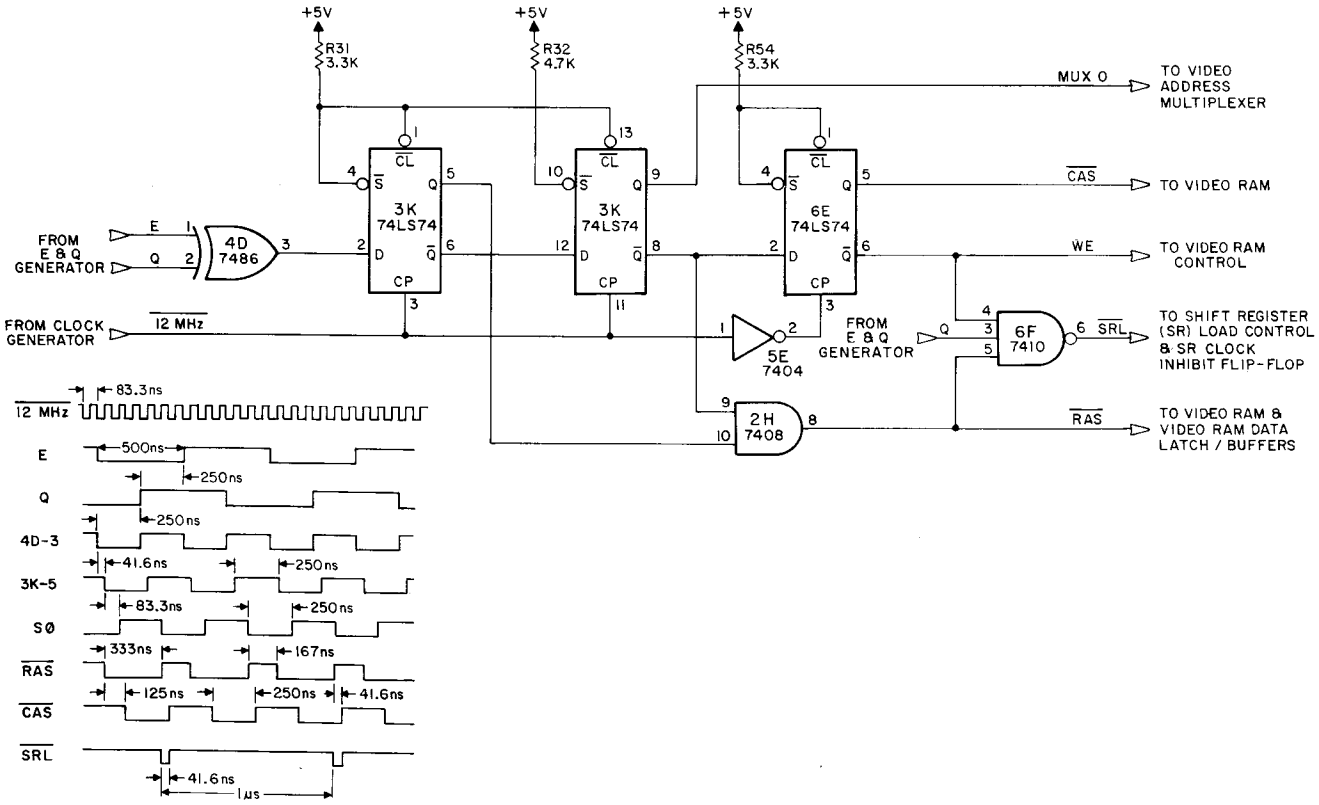


Figure 3-8. Video RAM Timing

Outputs of the 3K latches are gated to produce $\overline{RAS}$ (Row Address Select Not). As this function goes low (always during the low state of MUX 0, row addresses are latched into RAM. The $\overline{12\ MHz}$ clock is inverted to delay the 2 MHz signal from the second 3K latch by approximately 42 mSec, producing $\overline{CAS}$ (Column Address Select Not) and WE (Write Enable) signals. As function $\overline{CAS}$ goes low (always during the high state of MUX 1), column address bits are latched into RAM. The high state of WE causes the Video RAM Control Circuit to produce write-enable signals to the Video RAM during the MPU write operation to the Video RAM.

The Q Clock, function WE, and RAS are gated to produce function $\overline{SRL}$ (Shift Register Load Not). This function pulses low every microsecond to load data from the RAM into the shift register.

VIDEO RAM ADDRESS MULTIPLEXER (Figure 3-9)
This circuit multiplexes 14 video address bits; 8 MPU, and 6 pseudo-address bits, seven bits at a time, to provide row and column RAM memory address bits. Video, MPU, and pseudo-address bits are applied through multiplexer chips and selected with proper timing for the Video and MPU systems. Access is with the video system reading and refreshing the screen, the MPU system writing to define the Color Monitor display, and reading/writing from/to the portions of RAM that are off-screen and used for scratchpad memory. The multiplexer circuit consists of four dual 4-to-1 multiplexers. With MUX 0 and MUX 1 both low, PA8 through PA13 and A0 (applied to the I0 inputs of 3L, 3N, 30, and Q3) are placed on the MAØ through MA6 memory address bus. When function $\overline{RAS}$ (Row Address Select Not) goes low, MA0 through MA6 are detected into the RAMs. When MUX 0 goes high, MPU address bits A1 through A7 are placed on the MA0 through MA6 bus, and then latched into RAM when $\overline{CAS}$ (Column Address Select Not) goes low. This completes the addressing cycle for MPU access.

When MUX 1 goes high, video address bits VA0 through VA6 (MUX 0 low) and VA7 through VA13 (MUX 0 high) are selected and latched into RAM by the falling edges of $\overline{RAS}$ and $\overline{CAS}$.

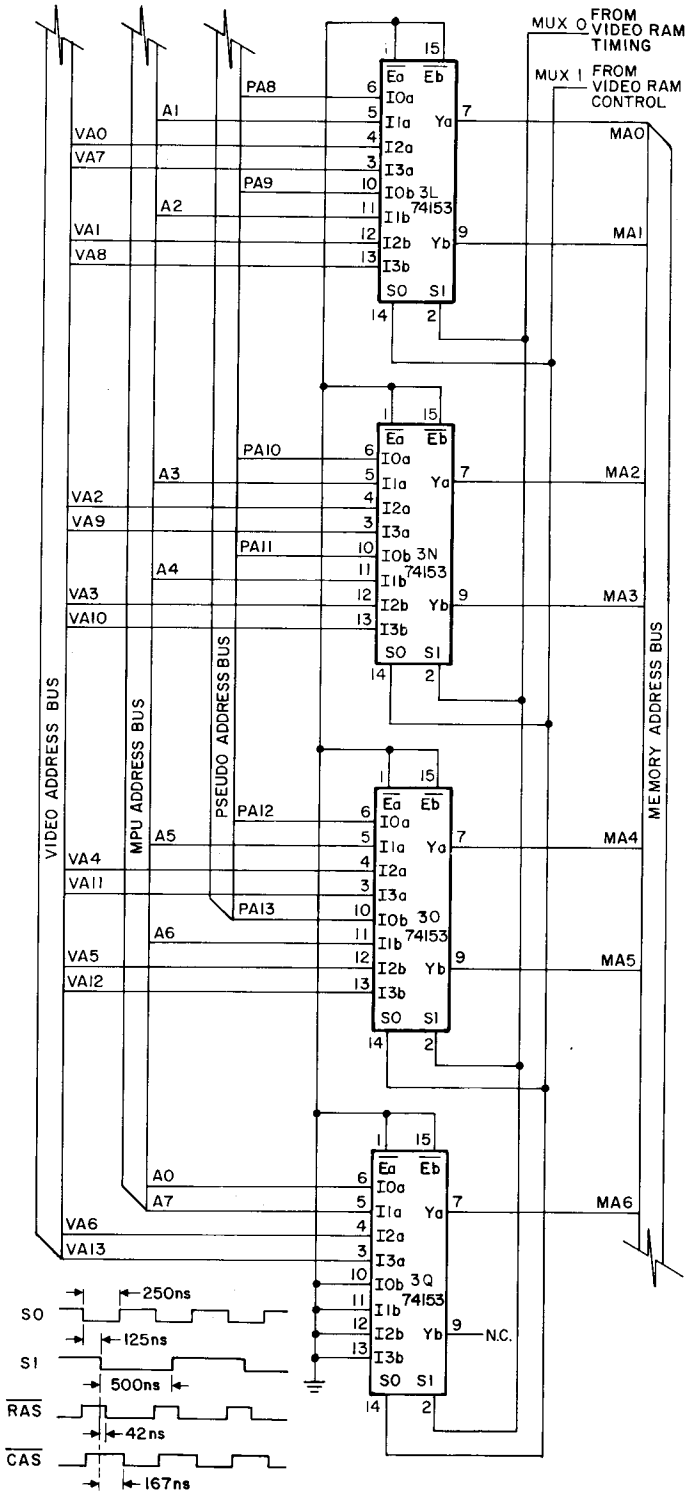


Figure 3-9. Video RAM Address Multiplexer

VIDEO RAM (Figures 3-10A and 3-10B.)
The Video RAM is provided by 3 banks of eight 16K-by-1 bit RAM chips. Seven address inputs on a memory address bus are used to access the memory locations. During video system access, the data outputs are loaded in shift registers to provide video information for the monitor. During MPU read operations, data is placed on the MPU data bus; during MPU write, MPU data from the MPU data bus is written into the RAM.

RAM Banks 1 and 2 are depicted in Figure 3-10A and RAM Bank 3 in 3-10B. RAM Bank 3 differs from RAM Banks 1 and 2 only in that data bits and write-enable functions for MPU write operations are supplied through the multiplexers. The state of the multiplex-select signal is always high, so Bank 3 is functionally identical to Banks 1 and 2. Because of this similarity, most of the discussion will be provided for Bank 1.

For an MPU read operation, row addresses are placed on the MA0 through MA6 bus and the falling edge of $\overline{RAS}$ (Row Address Select Not) latches the row address into the RAM. Next, column addresses are placed on the bus and the falling edge of $\overline{CAS}$ (Column Address Select Not) latches the column address bits.

Data is read out of all three RAM Banks. The rising edge of $\overline{RAS}$ clocks the RAM Bank Data Bus/bits D10 through D17, D20 through D27, and D30 through D37 into data buffers. Function $\overline{E1}$ (Enable 1 Not) from the Video RAM Control circuit is then applied to the OE (Output Enable) input of data buffer 4K, placing the Bank 1 Data Bus bits D10 through D17 onto the MPU Data Bus.

For an MPU write operation to Bank 1, the three RAM Banks are accessed as described for the read operation and data is read from Banks 2 and 3 onto the Data Bus bits D20 through D27 and D30 through D37. The Video RAM Control Circuit provides $\overline{WE1}$ (Write Enable 1 Not) and the MPU Data Bus D0 through D7 is written into RAM Bank 1.
For an operation concerning Bank 3, the D1, D2, D5, and D6 data bit inputs to multiplexer chips (6H) and the write-enable (WE3) input to multiplexer chip (6G) are permanently selected. This makes Bank 3 functionally identical to Banks 1 and 2. The two D3 and D7 data bit inputs, and the two Write-Enable-Not signals ($\overline{WE1}$, $\overline{WE2}$) are never selected. With a high $\overline{SMC}$, data bits D1 and D2 are presented to RAMs 6M and 6N, respectively. In likewise fashion data bits D5 and D6 are presented to RAMs 6Q and 6R. The $\overline{WE3}$ (Write-Enable-Not) signal is presented through multiplexer chip 6G to the write-enable inputs of RAMs 6M, 6N, 6Q, and 6R. Function $\overline{WE3}$ is connected directly to the write-enable inputs of RAMs 6L, 6O, 6P, and 6S.
Video system access to the RAM is the same as described for MPU access except that neither $\overline{E1}$ nor $\overline{WE1}$ is produced. Instead, the Video RAM Timing Circuit causes the three RAM Bank Data Busses to be loaded into shift registers. Note that during MPU access time, when the MPU is accessing addresses above RAM $C000_{16}$-$FFFF_{16}$, the video address bus accesses the RAM, but the RAM Bank Data Busses are ignored since $\overline{E1}$, $\overline{WE1}$, and the Video RAM Timing Circuit load signal are all inactive.

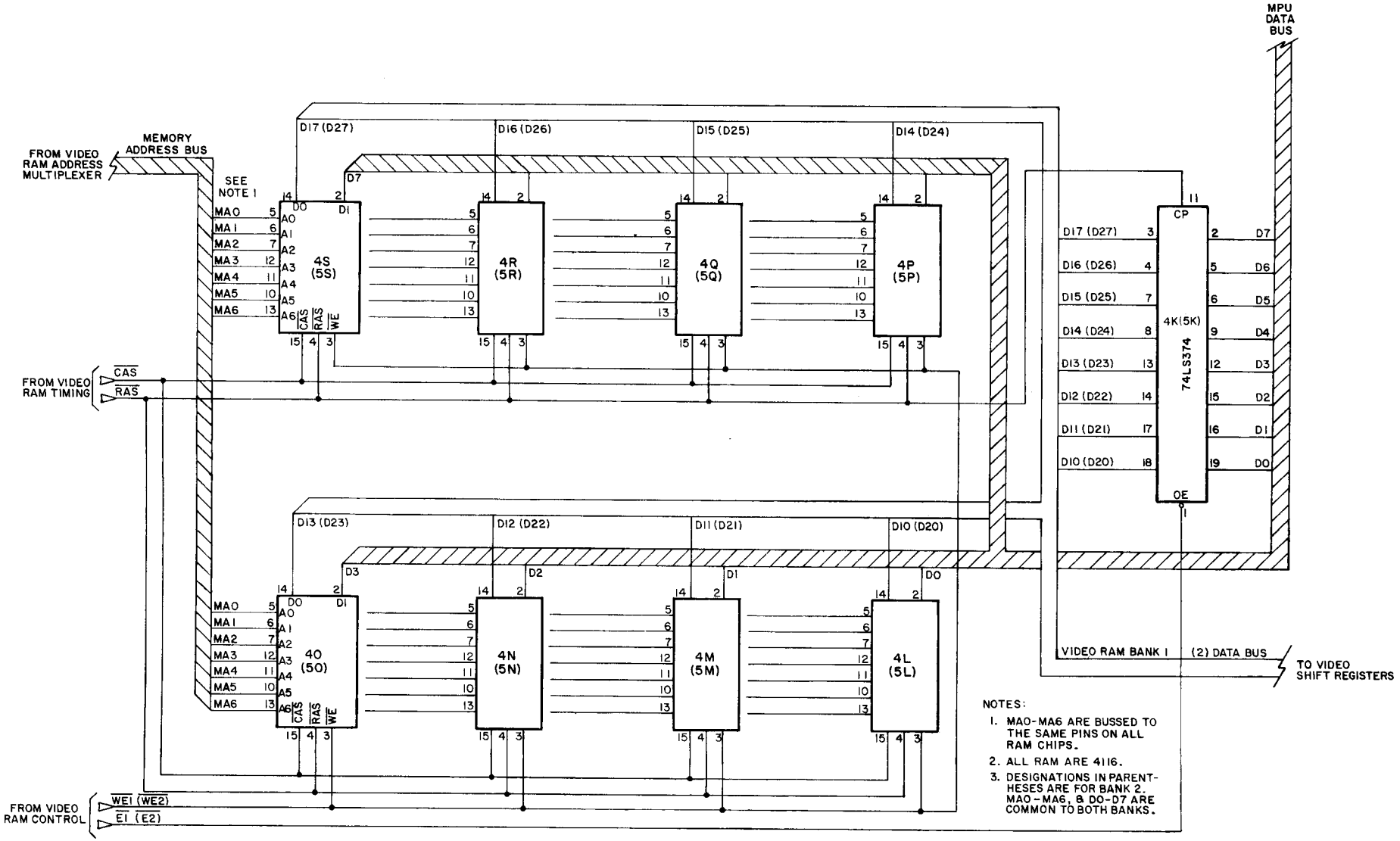


Figure 3-10A. Video RAM (Banks 1 and 2)

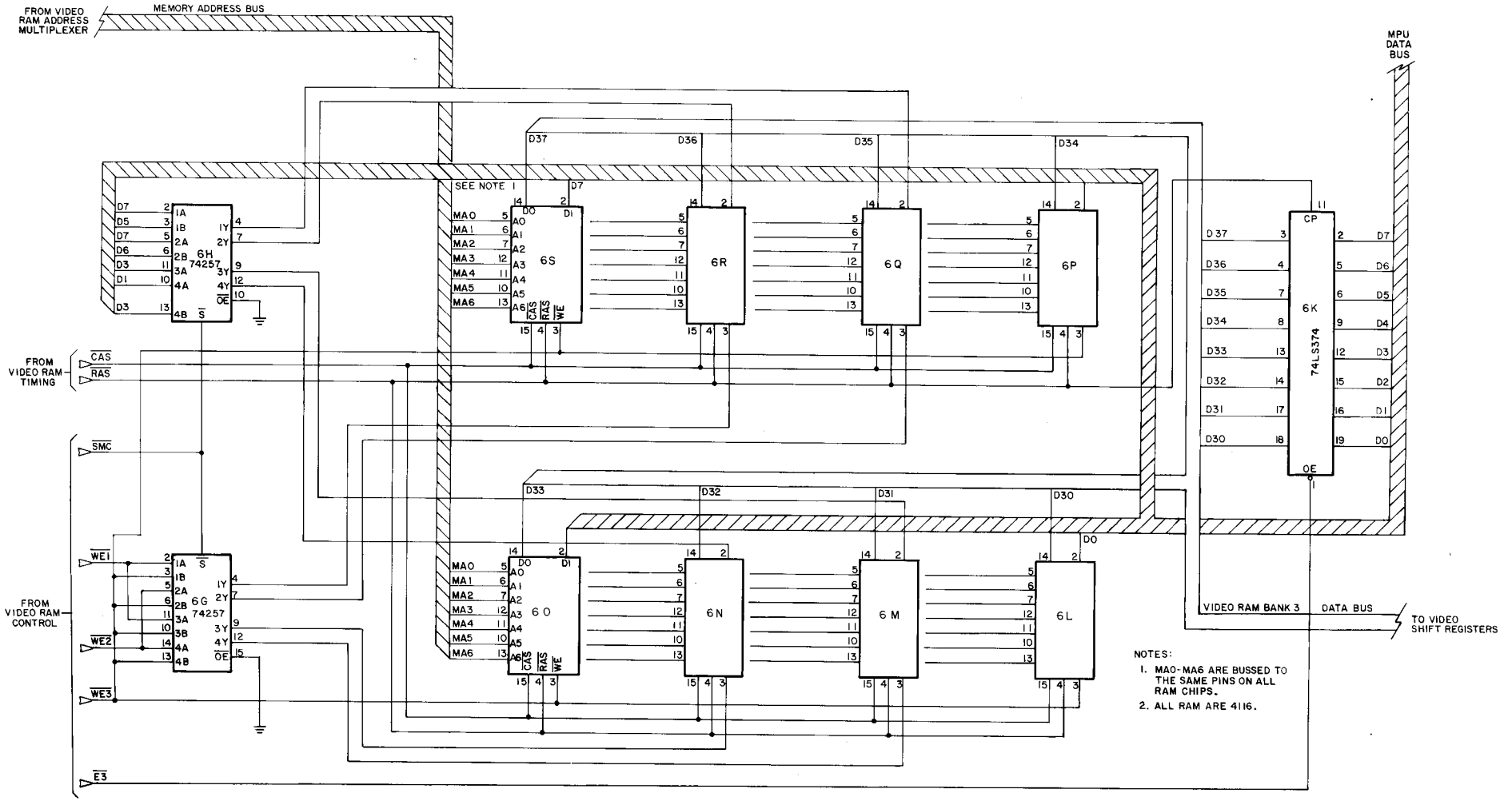


Figure 3-10B. Video RAM (Bank 3)

VIDEO SHIFT REGISTERS (Figure 3-11)

The Video Shift Registers convert the 24-line RAM Bank Data Bus into a 4-bit serial data flow. With information for six pixels (picture elements) on the RAM Bank Data Bus, a load pulse from the Video RAM Timing Circuit places the information into the shift registers and the 6 MHz clock shifts it out to the Color RAM Address Multiplexer.

When function $\overline{SRL}$ (Shift Register Load Not) goes low, the RAM Bank Data Busses are loaded into the shift registers. Function $\overline{SRL}$ also sets the 6E latch section to produce a high clock inhibit. The D14 through D17 bits loaded into the H inputs of the shift registers are available at the QH outputs.

The rising edge of the 4 MHz clock clears the 6E latch to permit the following rising edge of the 6 MHz clock to shift the D10 through D13 bits, loaded into G of the shift register, to the QH output. The following four 6 MHz rising edges, clock the D24 through D27, D20 through D23, D34 through D37, and D30 through D33 data bits to the QH output. After 1 microsecond, a new $\overline{SRL}$ pulse is produced to load the new data available from the next video system RAM access. This process is continuously repeated as a part of normal game operation.

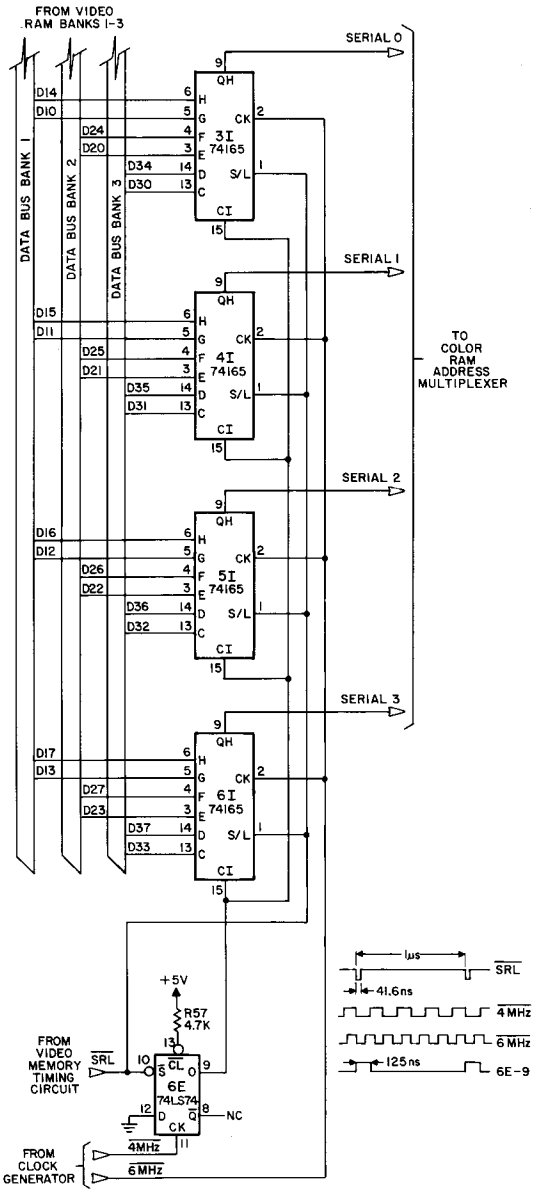


Figure 3-11. Video Shift Registers

COLOR RAM CIRCUIT (Figure 3-12)

The Color RAM is accessible to the MPU for storing data to define available colors for presentation on the Color Monitor. The circuit continuously accepts four lines of serial address information from the Video Shift Registers to access the color RAM and places the data out for digital-to-analog conversion to drive the red, green, and blue color guns of the Monitor. During intervals between horizontal traces when the serial information represents data from scratchpad RAM, a blanking signal inhibits the drive to the Color Monitor guns.

Functions $\overline{R}/W$ (Read Not/Write), $\overline{PSO}$ (Page Select 0 Not) from the Page Select Decoder (inverted to be PSO), and the E Clock are gated to provide a high to 5F and 5G gates. Function $\overline{E5}$ (Enable 5 Not), which corresponds to address $C000_{16}$ and MPU address bit A4 are gated with this high to produce a high WDFF (Watchdog-Flip-Flop) for address $C010_{16}$ or a low $\overline{WCR}$ (Write Color RAM Not) for address $C000_{16}$. WDFF is applied to the Watchdog Timer.
Function $\overline{E5}$ is applied to the color RAM address multiplexer to select MPU address bits A0 through A3. RAMs 1C and 1O are addressed with the low $\overline{WCR}$, and the state of the MPU Data Bus bits D0 through D7 is written into the addressed location.

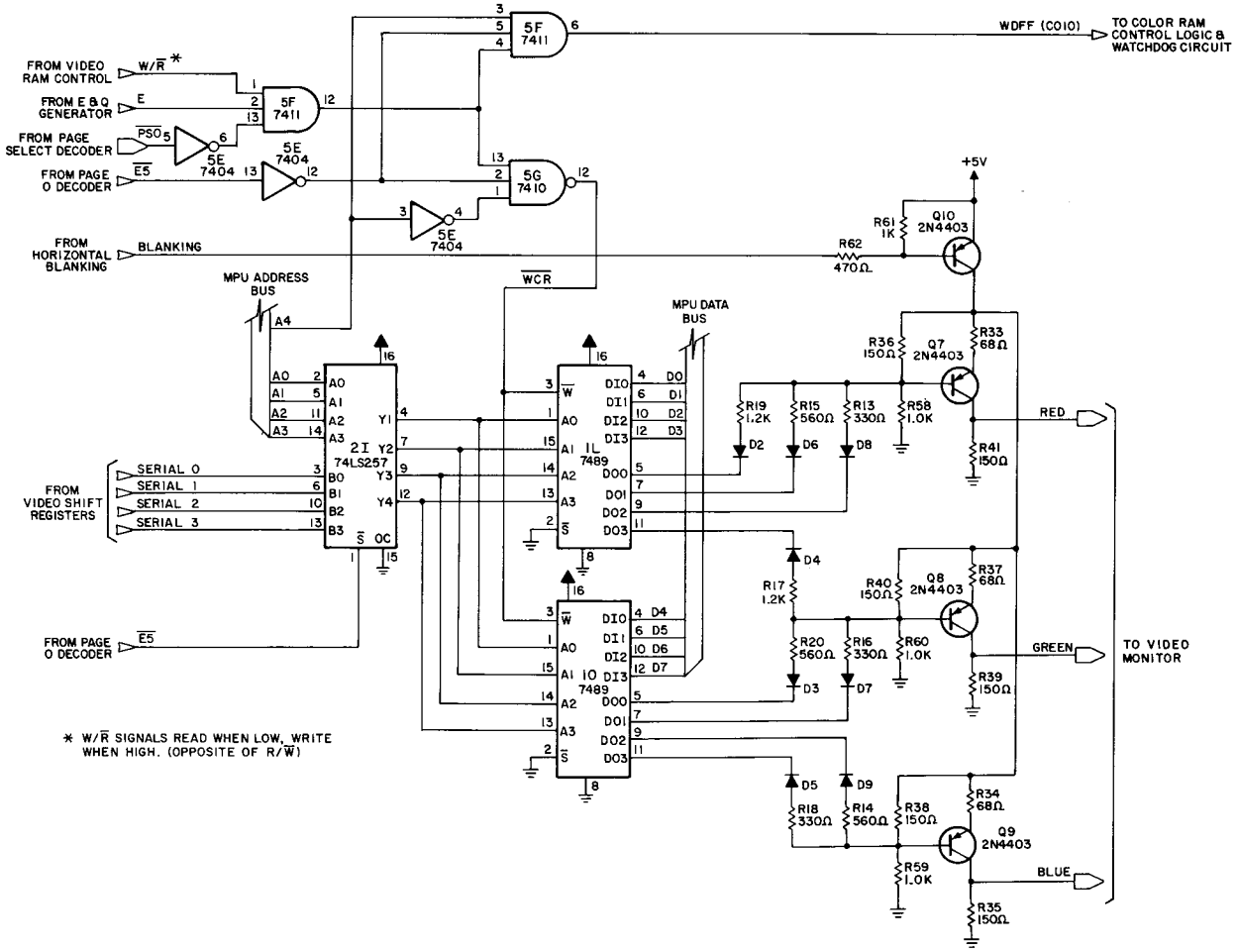


Figure 3-12. Color RAM Circuit

With $\overline{E5}$ high, Serials 0, 1, 2, and 3 are passed through the 2I multiplexer to RAMs 1L and 10 for reading. Data Output bits D00, D01, and D02 from RAM 1L are applied to a D-to-A converter for the red gun. With all three bits high, Q7 is cut off and no red gun drive is provided. A low D00 forward biases D2 to turn on Q7 for minimum red gun drive. Low outputs on D00, D01, and D02, and combinations of the three outputs forward bias D2, D6, and D8 for seven different intensity levels of red gun drive.

The green gun circuit is similar, using the 1L D03 and 10 D00 and D01 outputs. The blue gun circuit accepts the 10 D02 and D03 outputs to provide no blue gun drive with both outputs high and three intensity levels with either one or both outputs low.

During the intervals that the data on the serial busses represent scratchpad RAM, the BLANKING function goes high and cuts off Q10. This removes power from Q7, Q8, and Q9 and no drive is provided to the Color Monitor guns.

MONITOR SYNC GENERATOR (Figure 3-13)

Horizontal and Vertical sync pulse timing is derived from the video address bus, which advances to the next video address (1 count) every microsecond. The first Horizontal Sync pulse after the game is turned on starts at video address count 56, or 56 uSec after the Video Address Generator begins counting.

Horizontal Sync is a 4 uSec pulse which occurs once every 64 uSec at the 56th video address count (count 55) of each 64 count horizontal line. Vertical addresses VA3, VA4 and VA5 are high, and VA2 low, at horizontal count 55 of each line, causing horizontal sync to be asserted. When the horizontal count reaches 60, VA2 goes high, ending the horizontal sync pulse.

The Vertical Sync pulse is a 0.77 mSec pulse that occurs every 16.6 mSec. VA9 through VA13 are gated to produce a high vertical sync at vertical count 248. The pulse ends when the Video Address Counter reaches the all-zero count.

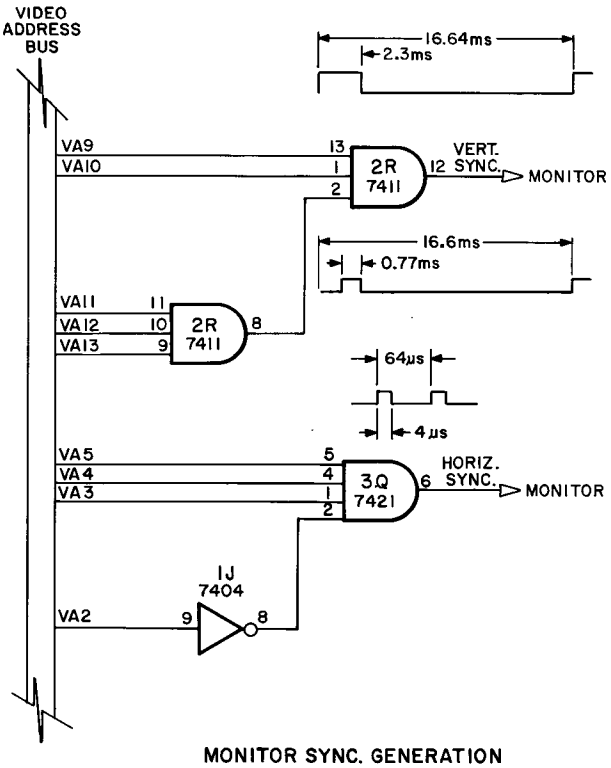


Figure 3-13 Monitor Sync Generator

BLANKING CIRCUIT (Figure 3-14)

This circuit is used to disable the video output to the Color Monitor when the memory section (scratchpad memory) outside the limits of the Color Monitor screen is being used.

Using video address bits VA0, VA2, VA4, and VA5, as inputs to a quad-input NAND gate contained in IC35, the blanking signal is activated (set high) when the video address bits are all high. This pulse remains high for 14 microseconds: the time it takes for address bits VA0, VA1, and VA5 to reach the proper states to cause pin 8 of IC35 to go low.

During this 14 microsecond period, the blanking key signal present at pin 6 of IC35 changes states nine times.

Both the blanking and blanking key signals then remain in ineffective states for a period of 50 microseconds. After this the entire cycle is repeated.

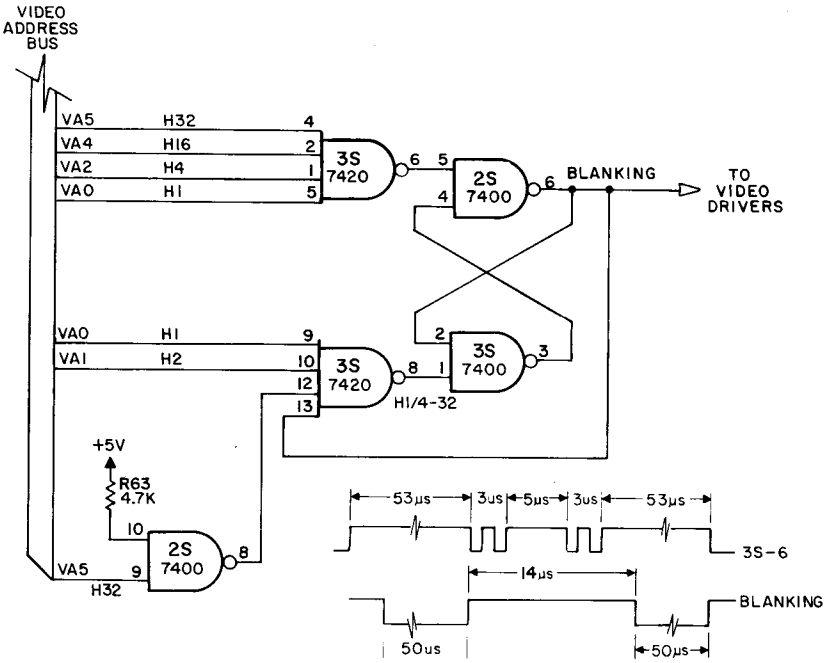


Figure 3-14. Blanking Circuit

PAGE 0 DECODER (Figure 3-15)

The Page 0 Decoder generates enable signals for MPU access of the color RAM, CMOS RAM, Vertical Count Buffer, and Interface Board PIA when Page 0 is selected. Function $\overline{PS0}$ (Page Select 0 Not) is asserted as long as Page 0 is selected, and $\overline{PE \cdot PS0}$ is asserted when the MPU accesses Page Selectable Memory (C000 through CFFF) with Page 0 selected. When the MPU accesses Page Selectable Memory (C000 through CFFF) with Page 0 selected, $\overline{PS0}$ and $\overline{PE \cdot PS0}$ are both asserted, enabling one-of-four decoder 2E. With A10 and A11 as inputs, each decoder output corresponds to a 1K segment of the page, and is asserted (low) whenever the MPU accesses an address within that 1K segment. The address shown on each output of the 74139 is the starting address of the 1K segment for which that output will be asserted. Function IPIA is an active high signal and is generated by using a 7427 NOR gate as a negative-logic NAND gate (output is high only when all inputs are low). Note that additional address decoding for the Interface Board PIA is provided on the Interface Board.

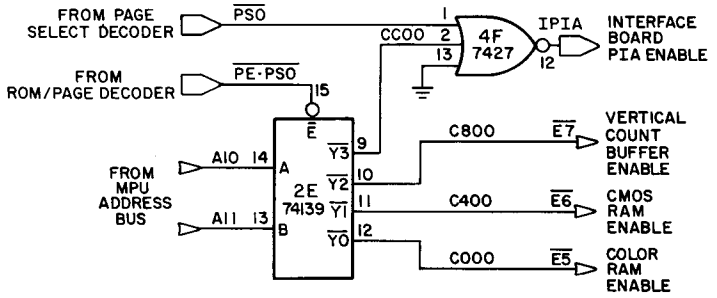


Figure 3-15. Page 0 Decoder

CMOS RAM (Figure 3-16)
The CMOS RAM has a standby power supply (B1, B2, B3) to save critical data while main power is off, and a memory protect circuit gating its R/$\overline{W}$ (Read/Write Not) input to protect the upper 128 locations from being changed while the coin door is closed. When the coin door is open, the data in the upper 128 locations of the CMOS RAM may be changed.

When the coin door interface switch is closed, a low is applied to inverter 1J, causing the MP (Memory Protect) signal to go high. Function MP will be low anytime the coin door switch is open or disconnected. Function MP is gated with MPU address bit A7 to produce a WI (Write Inhibit) signal which is asserted anytime the coin door is closed and the MPU is addressing any location from $C6ØØ_{16}$ to $C7FF_{16}$. Function WI is gated with the MPU R/$\overline{W}$ line to provide the CMOS RAM with a R/W signal which will not go low (write) for any of the upper 128 locations (C600 through C7FF) while the coin door is closed. When the coin door is open, MP is negated and no write signal is inhibited. If the MPU is addressing one of the lower 128 locations ($C400_{16}$ through $C5FF_{16}$), A7 will be low and a write signal is not inhibited at any time.

Two chip-enable inputs ($\overline{CE1}$, CE2) must be asserted to access the RAM chip. Function CE2 is asserted by $\overline{RESET}$, which is high during normal operation. $\overline{CE1}$ is asserted when both $\overline{E6}$ and $\overline{PSØ}$ are asserted, enabling the CMOS RAM for a data transfer when the MPU addresses any location from C400 to C7FF with Page Ø

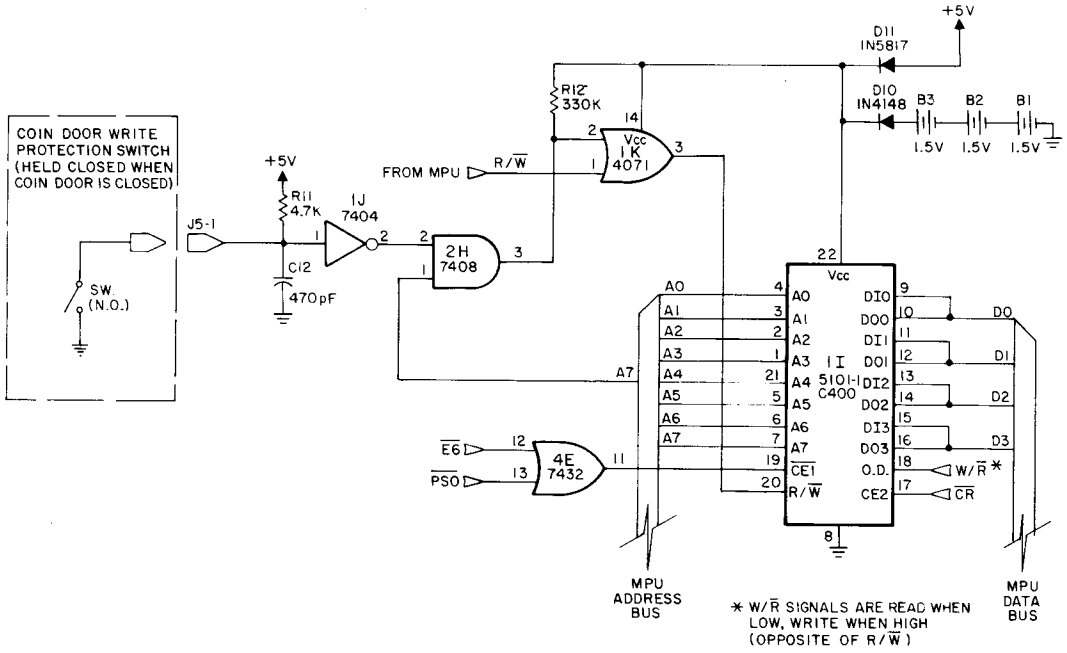


Figure 3-16. CMOS RAM

selected. Which of the 256 RAM locations gets accessed is determined by MPU address bits A0 through A7.
The RAM output buffers are disabled (tri-stated) by R/$\overline{W}$ when the MPU writes data to the RAM, and enabled when the MPU reads the RAM, thus allowing the RAM input and output bits to be tied together to the bi-directional MPU Data Bus with no drive conflicts. Data-transfers occur over MPU Data Bus bits D0 through D3, bits D4-D7 are ignored.

Diodes D10 and D11 form a switch that connects the CMOS RAM and gate 1K to the higher of the two supply voltages. When main power is on, current flows through D11 from the +5 power supply and D10 is reverse biased, isolating the standby batteries from the circuit. When the main power is turned off (or fails), and the +5VDC supply drops, D10 begins to conduct as its cathode reaches .7VDC below its anode, and holds the RAM Vcc at 3.8 VDC. The +5VDC supply continues to drop to 0V, causing D11 to become reverse biased and isolating the +5VDC supply line from the standby supply.

When the +5V supply has dropped to approximately 4.75 VDC the Reset circuit asserts CR, negating the CE2 input of the RAM and disabling any data transfers until the main power is on and stabilized. IC 1K and resistor R12 are also connected to the standby supply in order to prevent the R/$\overline{W}$ input of the RAM from going low (write mode) with power off.

VERTICAL COUNT BUFFER (Figure 3-17)
This buffer provides the program the ability to determine the vertical position of the scan on the monitor. When this circuit is accessed, the high-order 6 bits of the Video Address Bus are placed onto the MPU Data Bus. When the MPU reads from address CB00, the Page 0 Decoder provides a low E7 (Enable 7 Not). Function $\overline{E7}$ is gated with a low $\overline{PS0}$ (Page Select 0 Not) from the ROM Board to place a low on the enable inputs of buffer 2K. Video address bits VA8 through VA13 are then placed on MPU Data Bus bits D2 through D7.

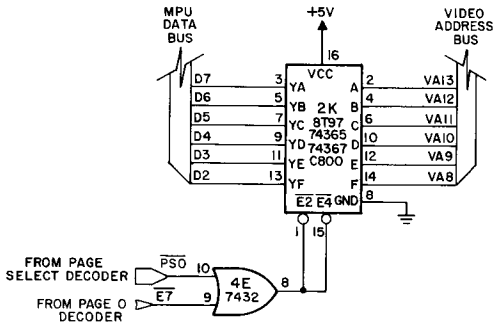


Figure 3-17. Vertical Count Buffer

COUNT 240 (Figure 3-18)
COUNT 240 produces an interrupt for the MPU indicating that the scan is at the bottom of the screen. COUNT 240 is applied to the PIA on the RAM Board to produce an interrupt for the MPU. When the video address reaches $15,360_{10}$ (Vertical Count 240), VA10 through VA13 are all high, causing COUNT 240 to go high. Since VA10 through VA13 remain high for all video addresses above $15,359_{10}$, COUNT 240 will be asserted for approximately 1.3 mSec (until the video address reaches maximum and starts again at zero). Since the screen is "scanned" or "refreshed" 60 times per second, COUNT 240 occurs at a 16.6 mSec rate.

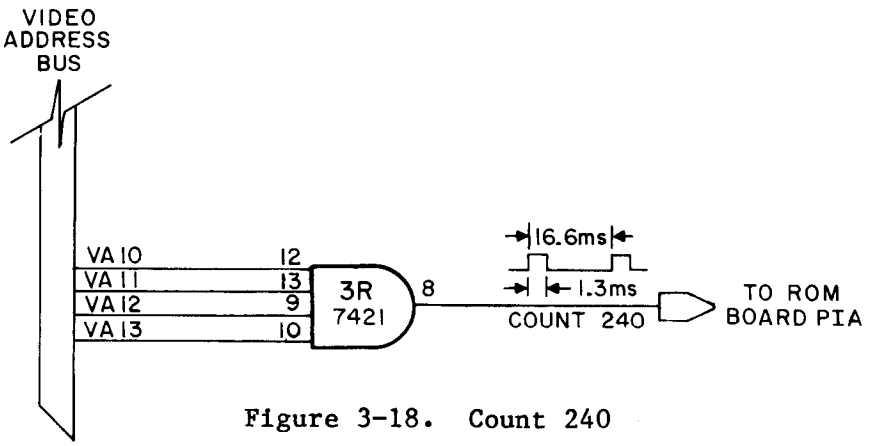


Figure 3-18. Count 240

ROM BOARD MEMORY SCHEME (Figure 3-19)

The ROM board in the DEFENDER game contains the main game program. Figure 4-1 shows a typical pair of memory devices used on the ROM board. The main game program requires that there be 4K memory locations present in or between IC1 and IC4, IC2 and IC5, IC3 and IC6 to contain memory sections labeled D, E, and F.

If IC1 is a 2K memory device, then IC4 must be a 2K memory device also to provide the necessary memory locations. When the memory section (D, E, or F) is split this way, the Upper/Lower ROM Decoder $\overline{LE}$ (Lower-Half Enable Not) is connected to pin 18 ($\overline{CS2}$: Chip Select 2 Not) of IC1 and the Upper/Lower ROM Decoder $\overline{UE}$ (Upper-Half Enable Not) connected to pin 18 ($\overline{CS2}$) of IC4. These signals select the memory section half (D000 or D800).

While the memory section half is being selected, the ROM/Page Decoder selects the memory section by supplying a $\overline{CS1}$ (Chip Select 1 Not) signal to pin 20 of each memory IC (IC1 and IC4) of the section (D) selected.

Note that jumpers W1 and W4 must be added when IC1 and IC4 are 2K memory devices. These jumpers are needed to make the pin 20 $\overline{CS1}$ connection common to both ICs and to connect the $\overline{UE}$ signal as required.

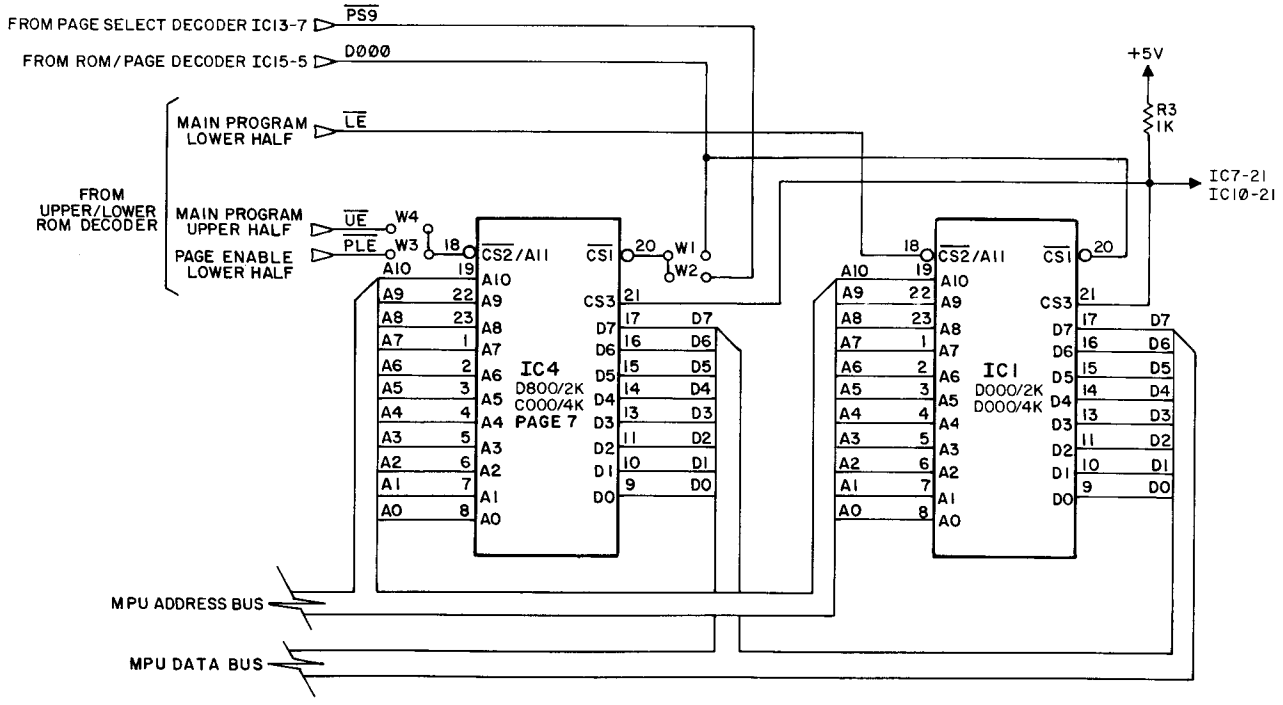


Figure 3-19. ROM Board Memory Scheme

When IC1 is a 4K device, IC4 can be used to hold extra game features. In this case, pin 18 of IC1 is address-bit 11 of the input address, and pin 18 of IC4 becomes the input for the $\overline{PLE}$ (Page enable lower half not) signal through jumper W3 from the Upper/Lower ROM Decoder. Also, pin 20 of IC4 is independent of IC1 pin 20, and is connected to the Page Select Decoder through jumper W2. Table 4-1 shows the two versions of DEFENDER currently available. Note that only version 2 has need for jumpers W2 and W4.

TABLE 4-1

IC	DEFENDER VERSION		MEMORY SECTION VERSION	
	1	2	1	2
1	4K	2K	D000	D000
2	4K	4K	E000	E000
3	4K	4K	F000	F000
4	-	2K	-	D800
5	-	-	-	-
6	2K	2K	C000/7*	C000/7*
7	2K	2K	C000/3*	C000/3*
8	2K	2K	C000/2*	C000/2*
9	2K	2K	C000/1*	C000/1*
10	2K	2K	C800/3*	C800/3*
11	2K	2K	C800/2*	C800/2*
12	2K	2K	C800/1*	C800/1*

* Memory Section/Page

ICs 6 through 12 contain memory block C000, and all pages thereof. Note that CS 3 (Pin 21) of each IC is tied high through resistor R1, R2, or R3 so that input is always enabled.

SECTION/PAGE SELECT DECODER (Figure 3-20)
This decoder provides page-enable signals PS0 through PS9 using MPU data bits D0, D1, D2, and D3. These four bits are BCD input signals to IC17, which, when clocked, presents these bits to pins 15, 14, 13, and 12 of IC13, a BCD-to-Decimal converter. IC17 is clocked when pin 10 goes low. This occurs whenever the E clock, R/$\overline{W}$ input from the MPU, and the memory section D enable signal ($\overline{Y1}$ of IC15) all go low. IC13 then provides an enable signal to 1 of 10 possible pages selected by the BCD input.

Memory section selections are made by IC15 and MPU address bits 15, 14, 13, and 12. Address bits 12 and 13 provide the selection input, and bits 14 and 15 (which activate once the address is above BFFF) provide a clock pulse from pin 8 of IC18 when both bits are high. If memory section E000 through EFFF is selected, and the MPU R/$\overline{W}$ signal goes low, the EDMA (Direct Memory Access Enable) signal is produced by IC14 and IC19. When page zero is selected by IC13 ($\overline{PS0}$), and memory section C is selected by IC15 ($\overline{PE}$), Pin 11 of IC16 goes low, effectively producing $\overline{PE} \cdot \overline{PS0}$ for input to the page zero decoder on the CPU/Video Board.

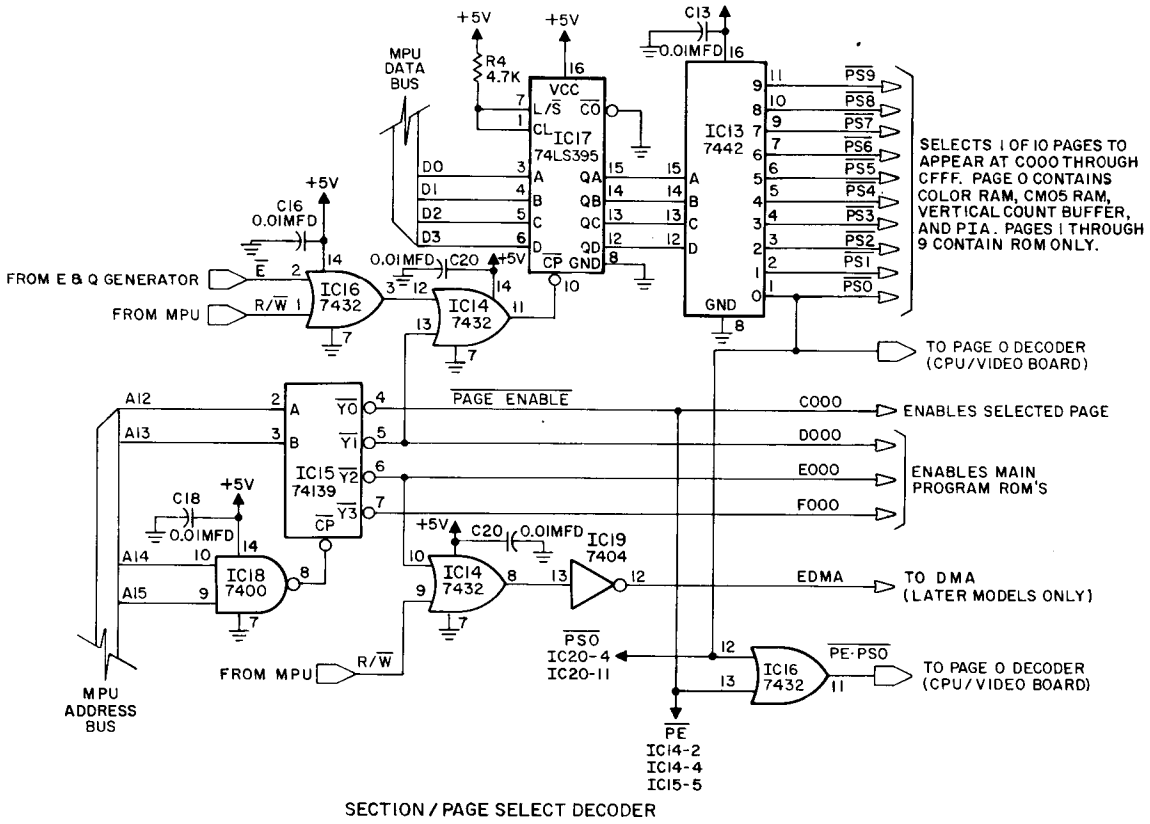


Figure 3-20. Section/Page Select Decoder

ROM SECTION/HALF DECODER (Figure 3-21)

This decoder uses the eleventh MPU address bit (A11) and the MPU R/W signal to determine the memory section half to be used by the main program. Also, the page-enable ($\overline{PE}$) signal from the Section/Page Decoder is gated with the section half-enable signal to produce a page-enable signal for the memory section half that is used.

When address bit A11 is low, IC19 presents a high to pin 5 of IC18. Then, when the R/W signal is high, the output of IC18 (pin 6) is a low ($\overline{LE}$), enabling the lower half of the memory section selected. This signal is then gated with the $\overline{PE}$ signal through IC14, and when both inputs are low the output of IC14 (Pin 6) provides a low ($\overline{PLE}$), which is the page-enable signal for the lower half of the memory section.

When address bit A11 is high and the MPU R/$\overline{W}$ signal is high, the pin 3 output of IC18 is a low ($\overline{UE}$), enabling the upper half of the memory section selected. This signal is then gated through IC14 as above to produce, at pin 3, ($\overline{PUE}$), the page enable signal for the upper half of the memory section selected.

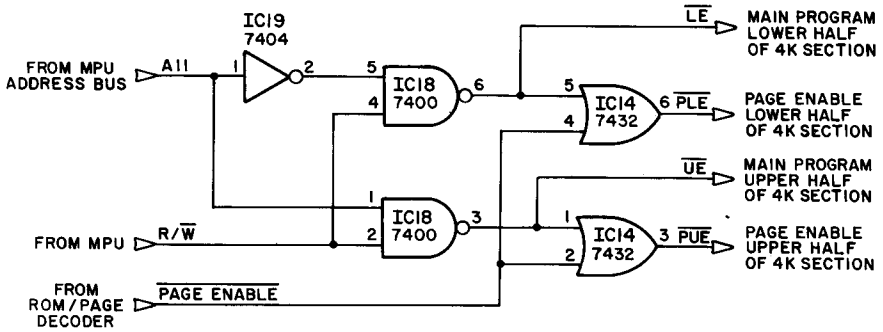


Figure 3-21. ROM Section/Half Decoder

ROM BOARD PIA/DECODER (Figures 3-22 & 3-23)

The PIA decoder uses inputs from the MPU address bus and the Section/Page Decoder. Address bits A10 and A11 are applied to pins 14 and 13 of IC15 respectively. A low output at Pin 9 ($\overline{Y3}$) is produced when A10 and A11 are both high (CC00) and $\overline{PE}$ (Page-Enable-Not) from the Section/Page Decoder is low. This $\overline{Y3}$ output is then gated with MPU address bit A4 and $\overline{PS0}$ (Page Select Zero Not) from the Section/Page Decoder to produce RPIA (ROM PIA) (address CC10).

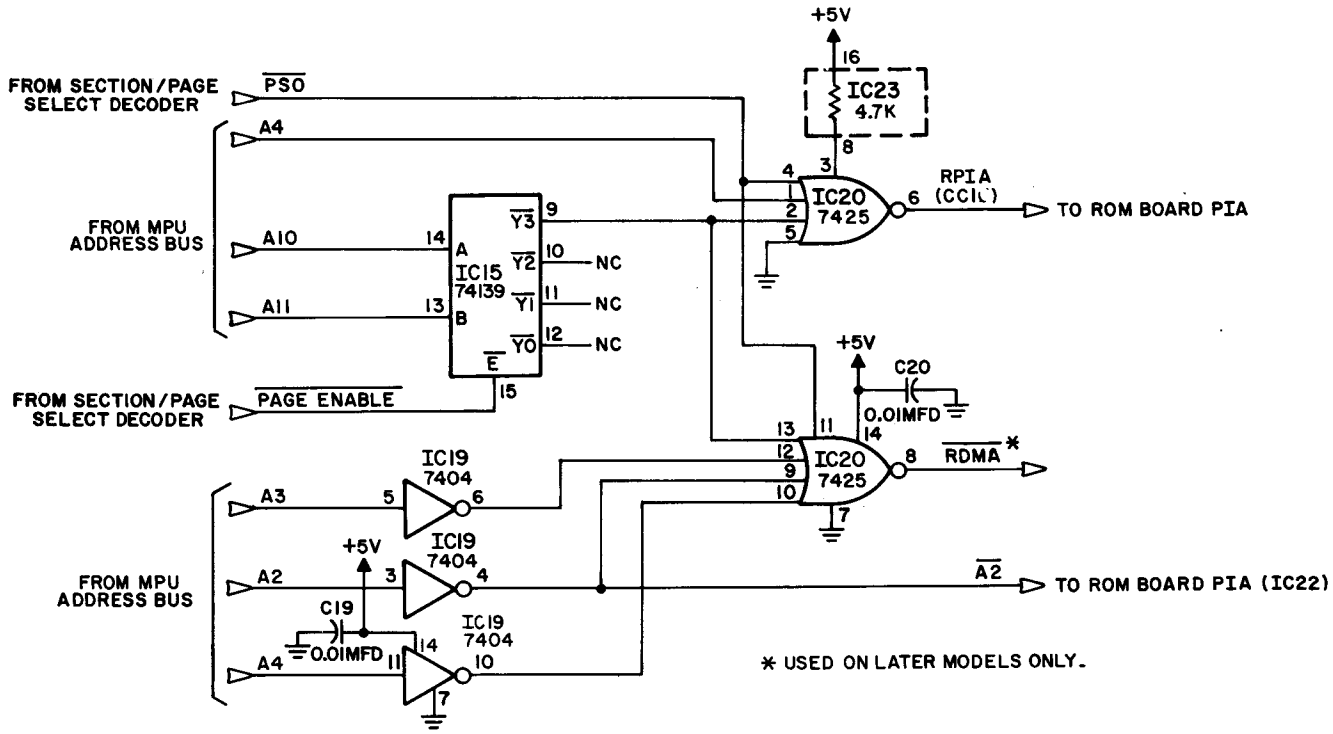
Address bits A2, A3, and A4 are inverted through IC19 and then gated with $\overline{Y3}$ through IC20 to produce the RDMA (ROM Direct Memory Access) signal.

The $\overline{A2}$ output of IC19 is gated through IC20, and applied to pin 24 of IC22 (CS1). The RPIA output of IC20 is applied to Pin 22 of IC22 (CS0). MPU address bit A3 is applied to Pin 23 of IC22 ($\overline{CS2}$).

Data bits 0 through 7 on the MPU Data Bus are used for, inputs from/outputs to, the coin door switches and sound module. Peripheral register A is used for coin door data and register B is used for sound module control. The program periodically reads register A and writes to register B to request sounds.

Inputs CA1, CA2, and CB1 from the Count 240 circuit, the coin door slam switch, and function VA11 from the video address generator. The negative-to-positive transition of any of these inputs cause $\overline{IRQA}$ & $\overline{B}$ (Interrupt Request Not) to go low. The MPU then reads the PIA to determine which input occurred. The CB2 lead is incorporated to provide "handshake" between the MPU chip on the Sound Board; this handshake is not implemented in DEFENDER.

MPU address bits A0 and A1 are applied to Pins 35 and 36 of IC22 for Register select zero and Register select one (RS0 and RS1) controls. The R/$\overline{W}$ signal from the MPU is applied to Pin 21 of IC22 and controls the direction of data flow through the PIA. The E input at Pin 25 of IC22 is the clock source for the chip. The Reset circuit input to the PIA at Pin 34 is used to clear the PIA registers when the game is being reset.



ROM BOARD PIA DECODER

Figure 22. ROM PIA Address Decoder

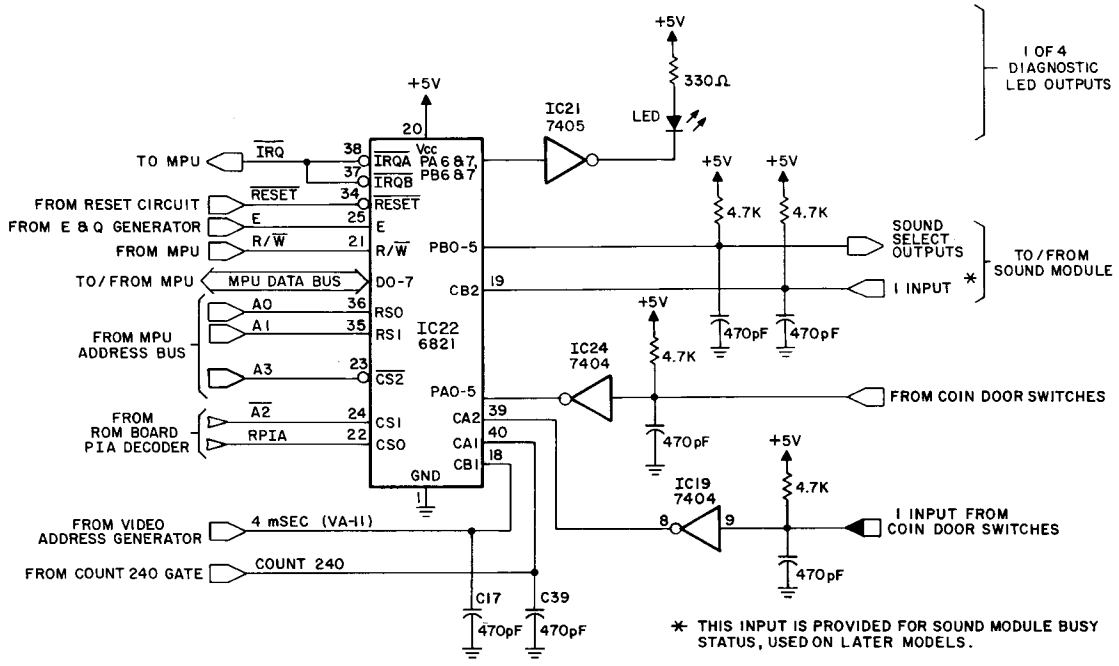


Figure 23. ROM Board PIA

INTERFACE BOARD ASSEMBLY (Figure 3-24)

Chip IC1, a PIA, is used to interface player switches with game circuits. MPU Data Bus bits 0 through 7 are used to connect the inputs to the MPU. The MPU R/W signal controls the direction of data flow. MPU address bit A3 is inverted through IC4 and applied to Pin 22 (CS0) of IC1. MPU address bit A2 is applied to Pin 24, CS1.

The IPIA signal from the Page 0 Decoder is inverted through IC4 and applied to Pin 23, CS2. MPU address bits A0 and A1 are applied to RS0 (ROM Select 0) and RS1 (ROM Select 1); respectively. The E clock is used to clock IC1, and the Reset Circuit input is at Pin 34.

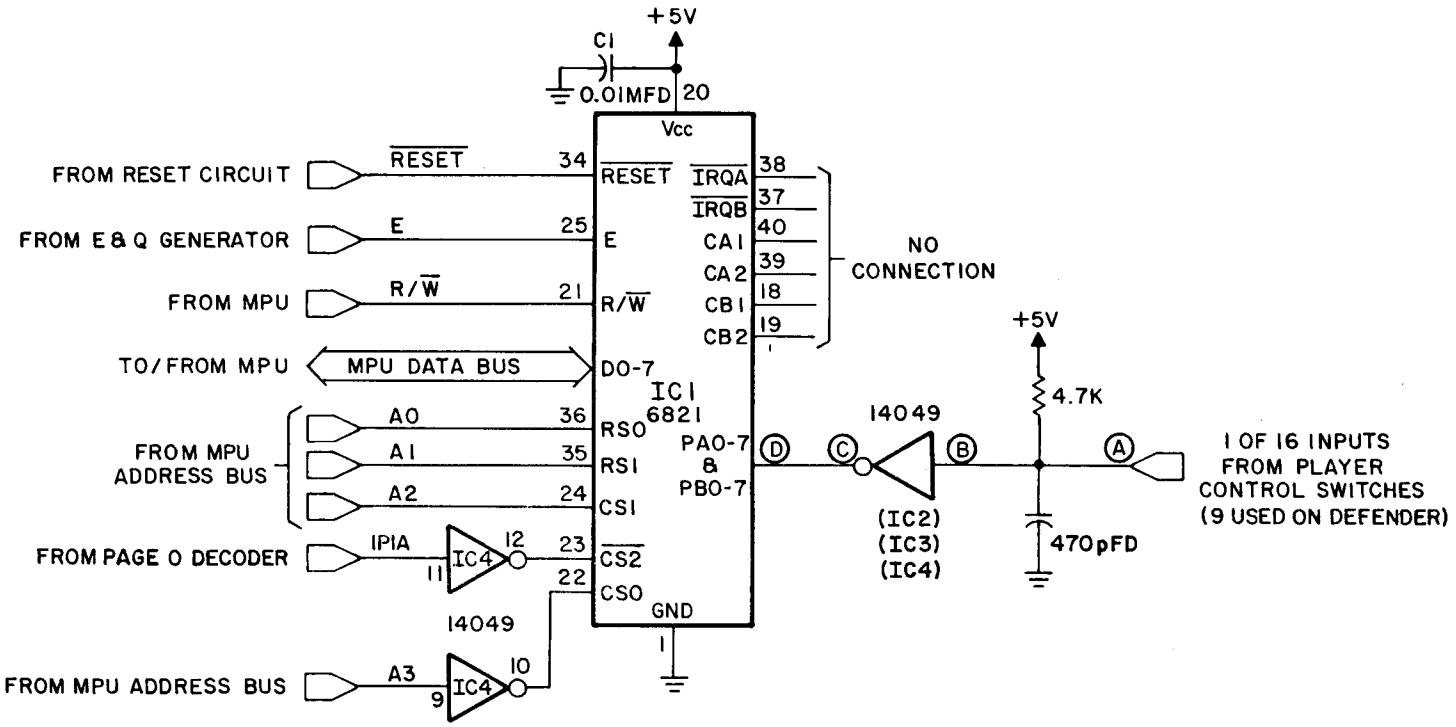


Figure 24. Interface Board Assembly

POWER SUPPLY

+5VDC Regulated, + 12,-12VDC Unregulated Supplies (Figure 3-25)

A transformer secondary provides a nominal 21.4VAC referenced to a center-tapped ground to 4J1. The AC is fused and applied across bridge rectifier BR1. A nominal -14.8 VDC (measured at TP3) is filtered by C6 and applied through 4J2 to the Sound Board for audio amplifier power. Similarly, a nominal +12.8 VDC (measured at TP2) is filtered by C12 and applied through 4J2 to the CPU/Video and Sound Board. The unregulated +12 VDC is applied to a power-on reset circuit on the CPU Board and provides amplifier power and an input to a 5-volt regulator on the Sound Board.

One leg of the AC input is applied to a voltage doubler consisting of C2-C3 and D2-D3 to provide a nominal +27.4VDC to regulator IC1. Resistor R1 and R2 provide the voltage reference of 5.1VDC at IC1-5; the values are critical. The V output at IC1-10 is applied to the base of the 2N6057 series regulator and the unregulated +12VDC to the collector to produce 5.1VDC (measured at TP1) which is applied through 4J2 to the CPU/Video, ROM, and (via the CPU/Video Board) the Interface Board.

With an increase of the +5VDC load, the drop across R6 would be greater and the output would tend to decrease. The voltage fed back to IC1-4 (inverting input) causes the voltage at IC1-10 to go more positive to maintain the +5.1 VDC output Similarly, a decrease in the load causes the IC1-10 voltage to go less positive.

The voltage divider consisting of R5 and R13 senses output current and at approximately 5A, applies a current limiting bias at IC1-2, dropping the IC1-10 voltage. If the load approaches approximately 6.2A, foldback current limiting occurs and the current through R6 is limited to approximately 1.3A. Therefore, a low voltage output with approximately 200mV dropped across R6 is an indication of an overload on one of the logic boards (CPU/Video, ROM, or Interface). Resistor R7 aids in the foldback current limiting and diode D1 provides temperature compensation for the current limiting.

LED 1 conducts through R16 to provide an indication of output voltage. Note, however, that should a circuit fault cause a high or low voltage, LED 1 may still be lit.

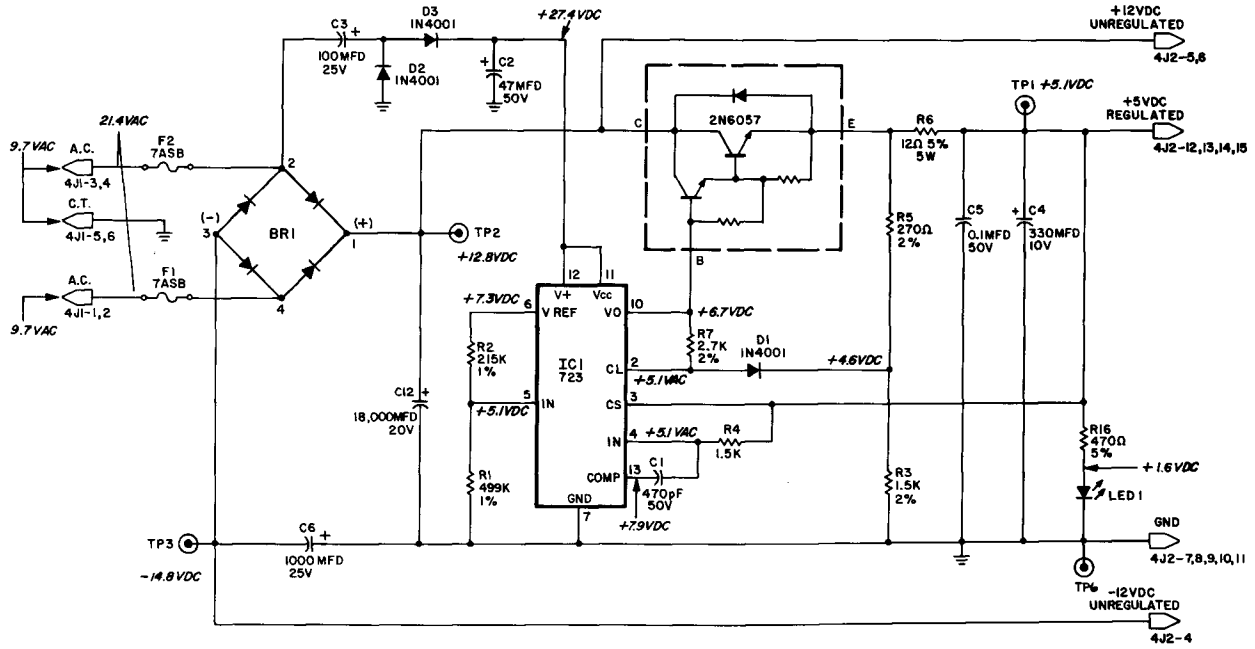


Figure 3-25. +5VDC Regulated, +12,-12VDC Unregulated Supplies

+27VDC Unregulated and +12VDC Regulated Supplies (Figure 3-26)

A nominal 20.9VAC from a transformer secondary is applied through 4J1 where it is fused and applied across bridge rectifier BR2. A nominal +26.6VDC is filtered by C13 and applied out 4J3 for power to the coin lockout relay. The +26.6VDC is also applied to regulator IC2 and pass transistor Q1. The 12.1VDC output (measured at TP4) is applied through 4J2 to RAMs on the CPU/Video Board.

The voltage divider consisting of R9 and R10 provides both a reference voltage and feedback to the inverting input at IC2-4. The V output at IC2-10 is applied to the base of Q1, establishing +12.1VDC at TP4. With an increase of the load on the +12VDC, the voltage at IC2-4 tends to go less positive which increases the voltage at IC2-10 to maintain the output voltage. Similarly, a decrease in the load causes the IC2-10 voltage to decrease.

The voltage divider consisting of R11 and R13 sets a current limiting bias of approximately 1A. Should the load increase to approximately 1.3A, foldback current limiting goes into effect and the voltage at IC1-10 is dropped to a level to allow only approximated 50 mA of current through Q1. Therefore, a low voltage output with approximately 15mV dropped across R14 is an indication of an overload on the CPU/Video Board.

Resistor R8 provides temperature compensation. LED 2 conducts through R17 to provide an indication of output voltage. Note, however, that should a circuit fault cause a high or low voltage, LED 2 may still be lit.

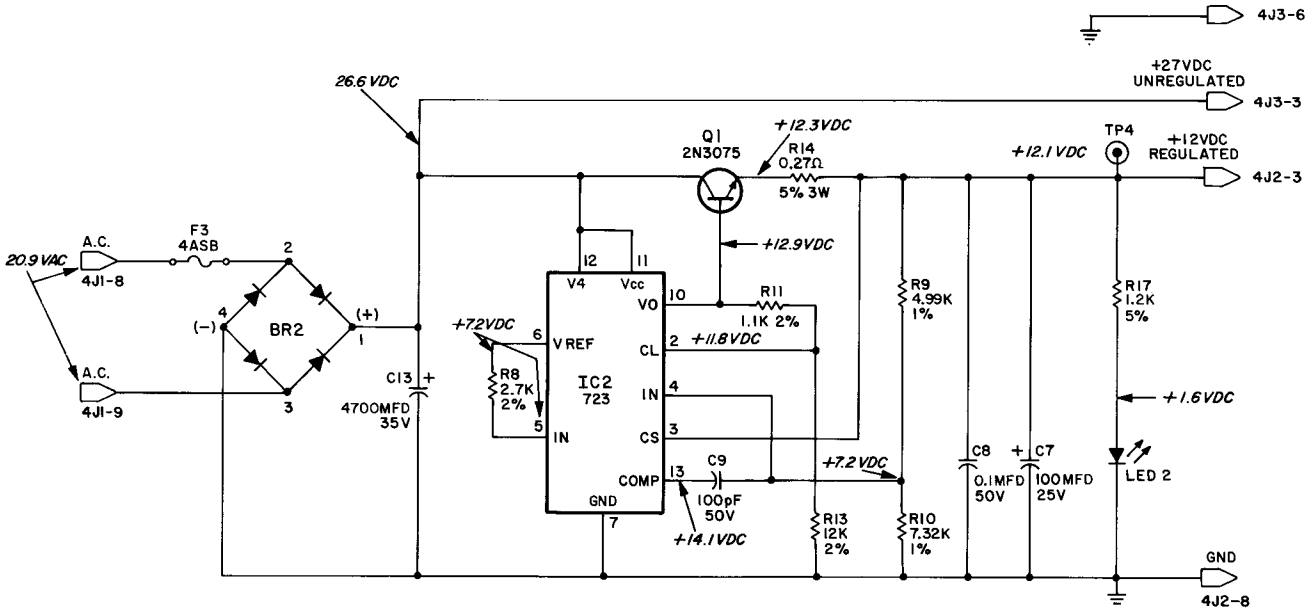


Figure 3-26. +27VDC Unregulated and +12VDC Regulated Supplies

-5VDC Regulated, 6.3VAC Supplies (Figure 3-27)

A nominal 9.1VAC from a transformer secondary is applied to 4J1. One line is fused and the two lines are applied out 4J3 for general illumination power. On cocktail table games, jumper W1 is open and R15 drops the AC voltage to a nominal 6.3VAC. On upright games, jumper W1 shorts R15 and a dropping resistor on the power panel lowers the AC voltage.

A separate fuse is in one line and the two lines are applied across bridge rectifier BR3. A nominal 10.4VDC is produced and filtered by C14. The Q2 voltage regulator provides a -5, + or -0.2VDC output (regulation to within 50mV) to RAMs on the CPU/Video Board. The regulator incorporates internal current limiting and will drop the output voltage to -1.1VDC with a short-circuited load.

LED 3 conducts through R18 to provide an indication of output voltage. Note, however, that should a fault cause a high or low voltage, LED 3 may still be lit.

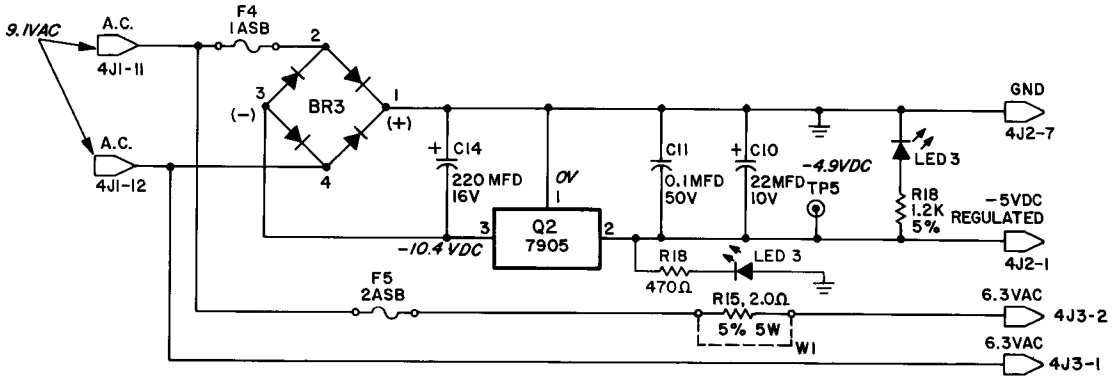


Figure 3-27. -5VDC Regulated, 6.3VAC Supplies